AMPHENOL AEROSPACE

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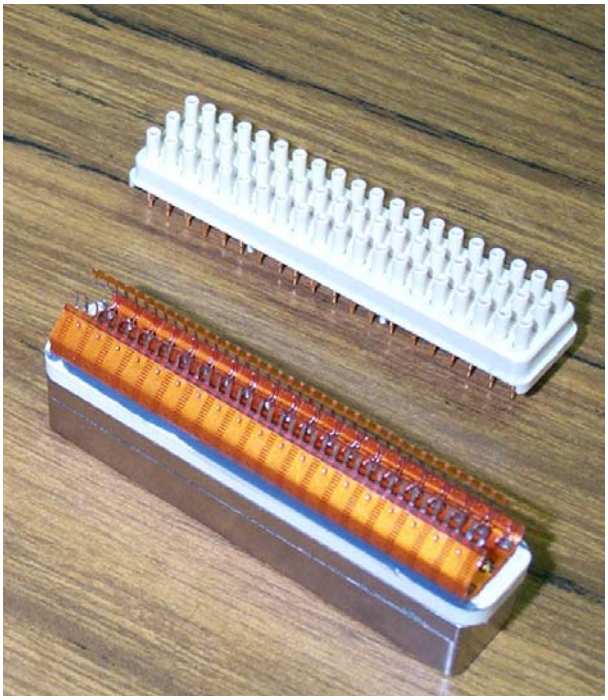
100 OHM DIFFERENTIAL PAIR INSERT PROJECT

ELECTRICAL CHARACTERISTICS MODELING AND PERFORMANCE TESTING



100 OHM DIFFERENTIAL PAIR INSERT PROJECT

ELECTRICAL CHARACTERISTICS - MODELING AND PERFORMANCE TESTING

OVERVIEW

This report contains the SPICE model of Amphenol's Staggered Grid LRM, 100 Ohm Differential Pair connector, which was developed via electromagnetic modeling techniques. Using the SPICE model, simulations of the electrical performance of the connector were conducted for several risetimes. The SPICE model accuracy was verified by testing a connector sample with a Time Domain Reflectrometer (TDR). The testing showed the differential impedance to be approximately 112 ohms at a 35 ps risetime; it is assumed that this will be pulled down to 100 ohms by capacitive discontinuities at the transition of the connector to the printed circuit boards. The crosstalk was a maximum of 9% at 35 ps risetime.

After the initial release of this report, a method of simulating Eye Diagram testing with the SPICE model was explored; the results of which can be found in Addendum 1. Simulations indicate that the mated pair of connectors is capable of conducting data rates of more than 2 Gbps. In addition, the simulations show that the discontinuities at the transition from the connectors to the printed circuit boards play a major part in data rate capability, which was in agreement with many other published papers regarding high data rate interconnects.

BACKGROUND

This project originally started as an attempt to achieve twenty 150 ohm differential pairs in the standard Amphenol LRM connector staggered grid insert. This proved to be impossible under the constraints of overall envelope, contact diameter, and insert dielectric properties. The requirement was eventually changed to twenty, 100 ohm differential pairs.

In order to accomplish this, the contact diameter was effectively reduced by substituting a dielectric material for the metal sleeve protecting the exposed portion of the brush contact, and by substituting a variation of the existing insert material with a lower dielectric constant.

DETAILS OF MODELING AND SIMULATION

Various geometry configurations were examined using a 2D static field solver to determine optimum contact spacing to achieve the desired differential impedance of 100 ohms. These initial efforts were made with the assumption that the insert would be populated with differential pairs only. (No ground contacts.) In other words, there was to be no single ended, 50 ohm to ground reference; each contact of the pair would be referenced to its mate. Under certain circumstances, a somewhat higher density might be achieved by referencing each pair to a separate ground contact. This was eventually changed at customer request, and a ground pin for each differential pair was added.

Due to manufacturing constraints, the physical design of the differential pair insert was broken down into an assembly of separate, "mini" inserts. Figure 1 shows two such "mini-inserts" side-by-side. Each differential pair exists between the outer contacts (upper and lower as shown in Figure 1) of two adjacent "mini-inserts". This was done to minimize skew as the electrical contacts transition to the impedance controlled flex circuit on the LRM connector.

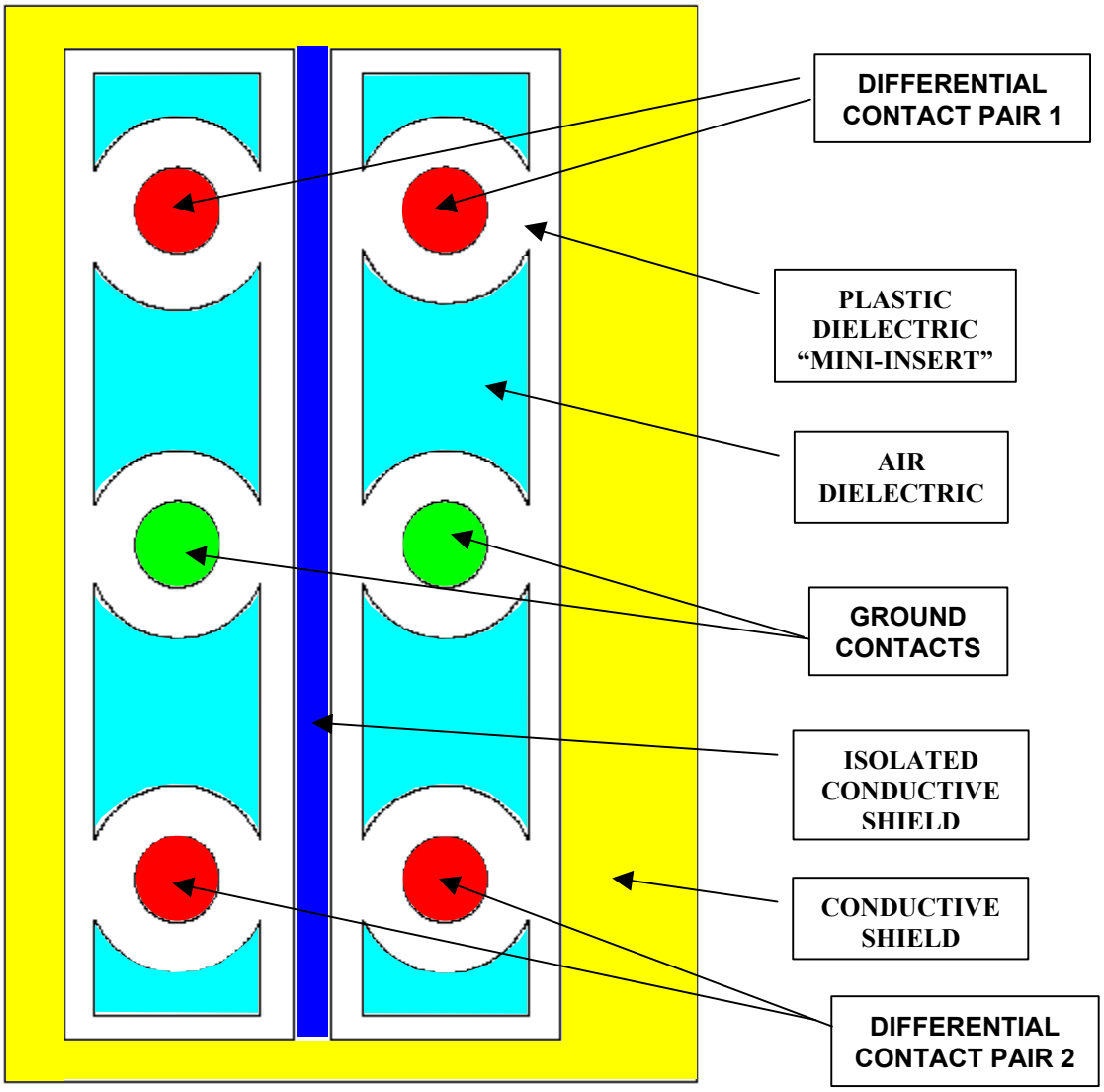


Figure 1. Schematic of the differential pair connector insert.

The EM Field Solver used was "PC Superfish", a group of codes that include a 2-D electrostatic and magnetostatic field solver, distributed by The Accelerator Code Group at Los Alamos National Laboratories.

Results based on the configuration shown in Figure 1 yielded good results for differential impedance, but higher than desired single ended (50 ohm) impedance. The reason for this being the shield surrounding each insert module is by necessity floating, rather than being grounded. Single ended impedance ended up at 63 ohms.

DIFF PAIR - FINAL MODULE DESIGN 5/9/00

L matrix (Henries)

0.611438E-08 -0.123820E-08

-0.124467E-08 0.618373E-08

C matrix (Farads):

0.160688E-11 0.321753E-12

0.323434E-12 0.158886E-11

Physical Length = 0.662000 inches

Propagation Delay = 0.991214E-10 seconds

Z matrix: (Ohms):

62.9828 12.7544

12.8210 63.6970

Zdiff = 100.457 ohms

Xtalk @ 50 ps = 10.0%

Xtalk @ 150 ps = 8.0%

Xtalk @ 300 Ps = 4.5%

The L matrix (inductance in Henrys) is defined as follows

L11 L12

L21 L22

where L11 is the inductance of pin 1 with all other pins grounded, L12 is the mutual inductance from pin1 to pin 2, L22 is the inductance of pin 2 with all other pins grounded, and L21 is the mutual inductance from pin 2 to pin 1.

The other matrices follow the same pattern. Z11 and Z22 are the single ended impedances, and Zdiff is the differential impedance of the pair. The reason Z_single-ended is not 1/2 of Zdiff,(i.e., 50 ohms) is the strong coupling between pins. This would be eliminated if the shields could be grounded, rather than floating. (A grounded shielding system would also eliminate any crosstalk; however, this would be mechanically impossible in the current design.)

These L and C values were then used to create a SPICE model (see Figure 2).

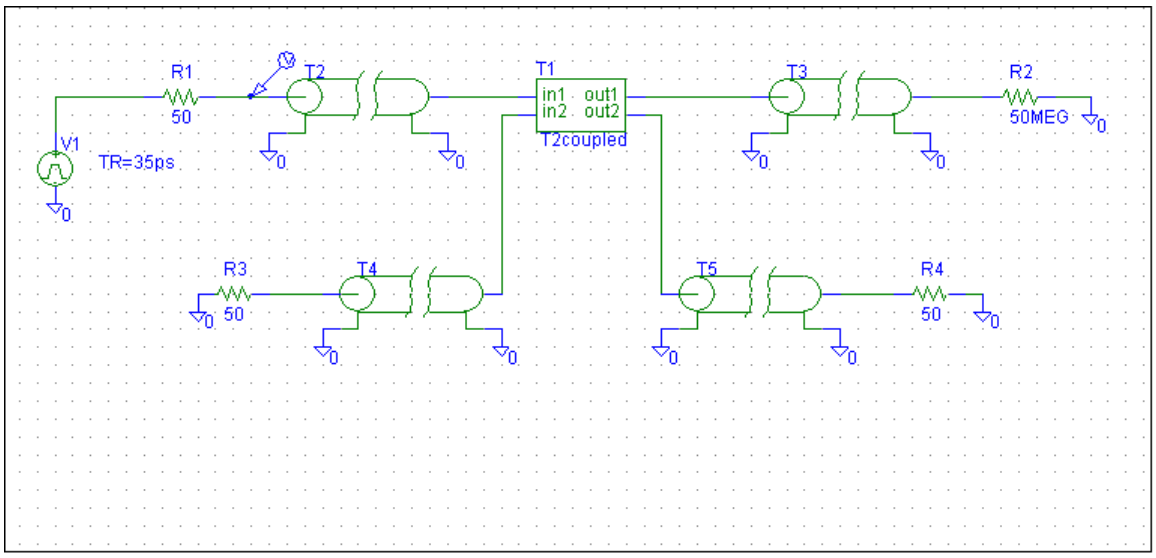


Figure. 2 SPICE model of the differential pair.

In Figure 2, T1 is the SPICE model for a coupled transmission line. The L and C values are entered into the model description, allowing both the Characteristic Impedance of the contact under test and crosstalk to the adjacent contact to be examined.

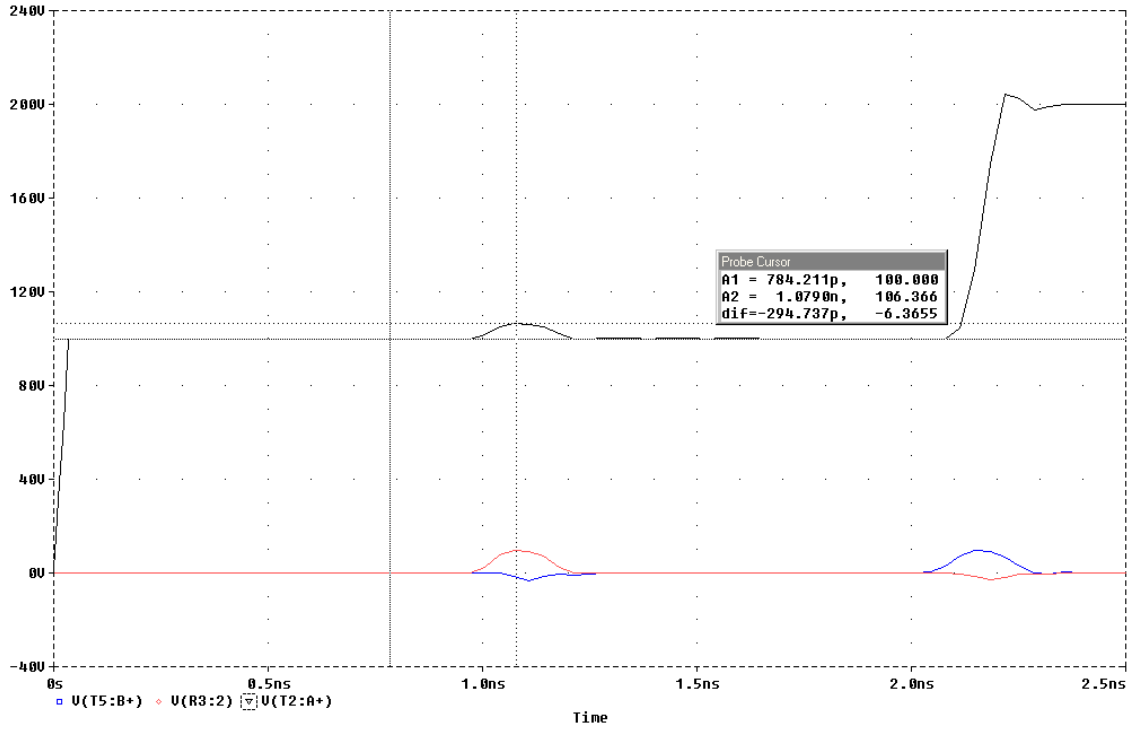


Figure 3. Differential Zo, Near End Xtalk, Far End Xtalk.

The upper trace of Figure 3 shows the active line, and the y-axis is scaled to read impedance in ohms. The cursor shows the pin at 106.4 ohms.

Figure 4 shows measured values for Near End Xtalk (NEXT) of 9.7% and Far End Xtalk (FEXT) of 3.4%. These values are based on a 35 picosecond risetime, equating to a 10 GHz bandwidth. A more realistic bandwidth of 1 GHz (350 ps) gives NEXT = 3.85%, and FEXT = 0.8%.

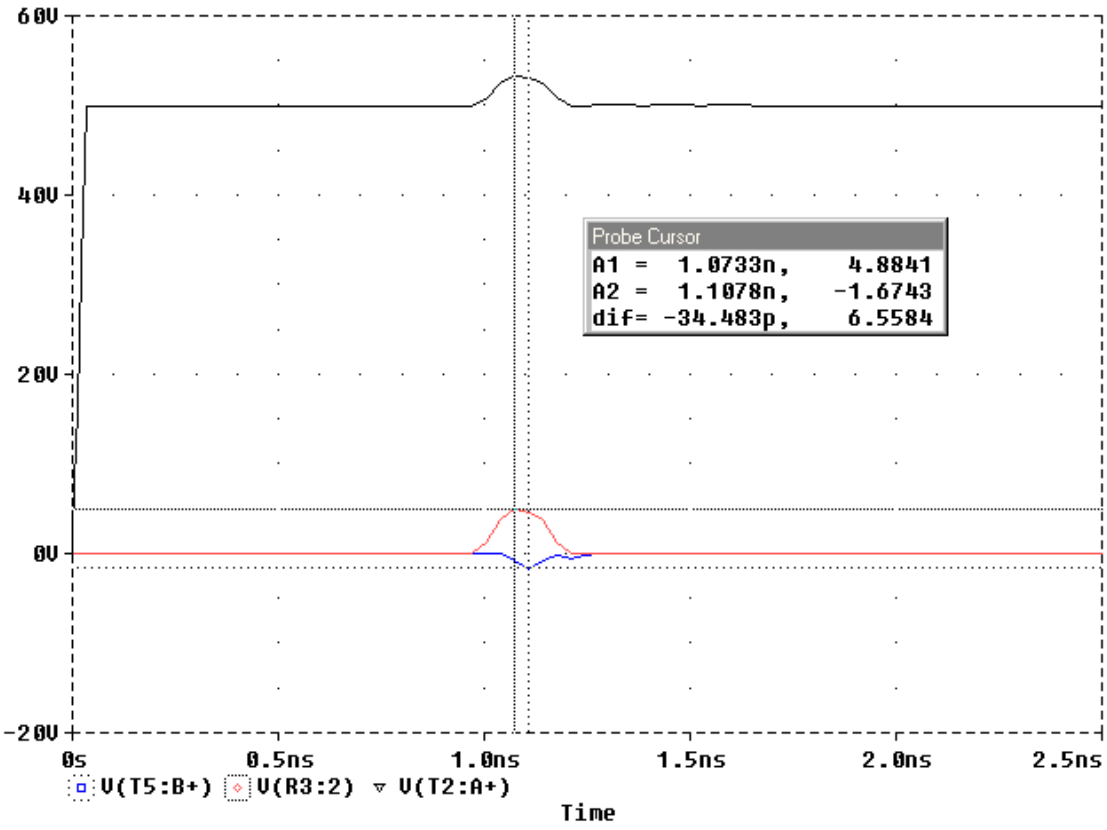


Figure 4. Near end and Far end crosstalk at 35picosecond risetime pulse.

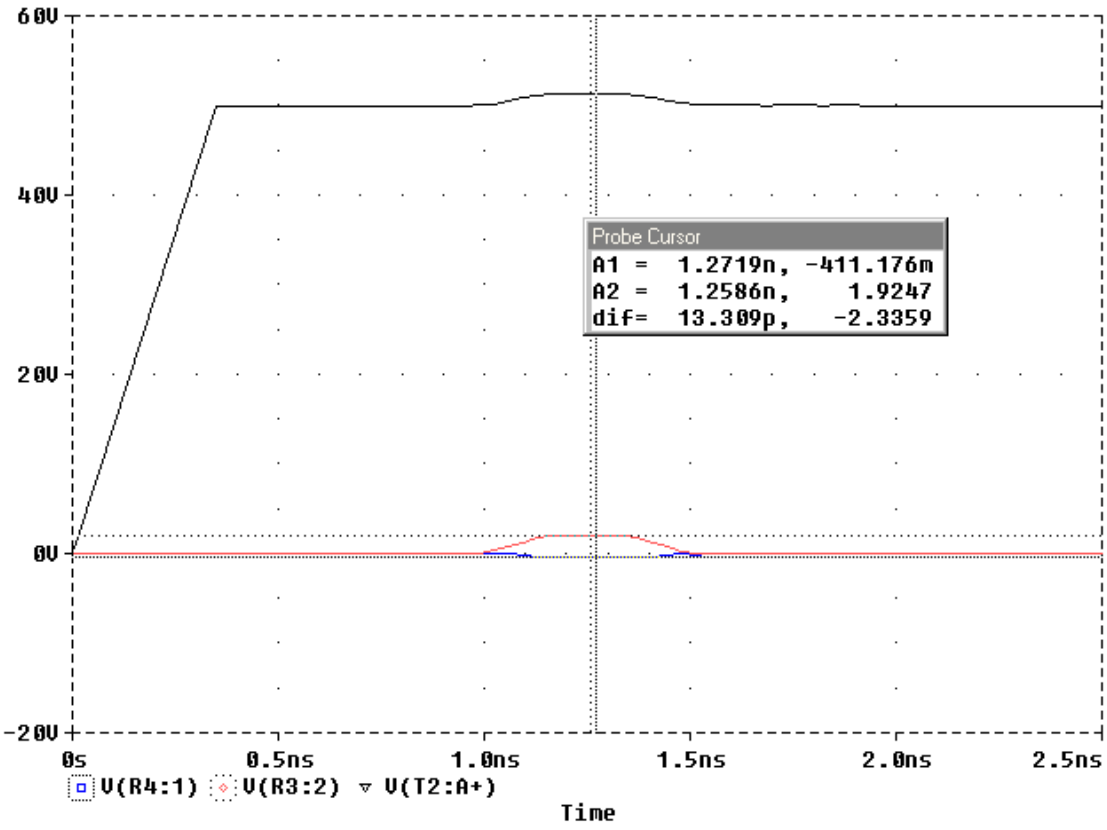


Figure 5. Near end and Far end crosstalk at 135 picosecond rise time.

Prototype connectors using this design concept have been built and tested using custom fabricated flex print test boards. (See Figures 6 and 7)

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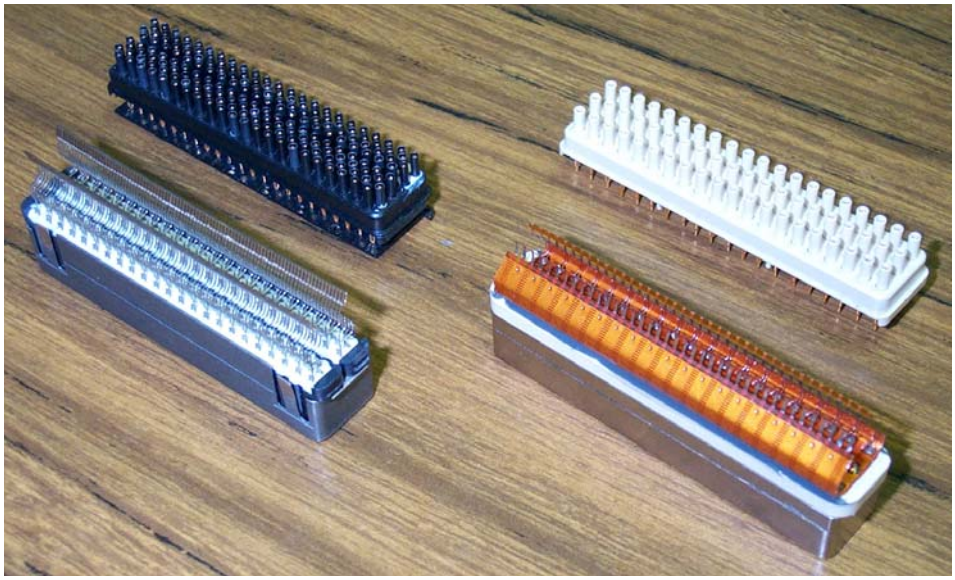


Figure 6. Standard Staggered grid 180 contact inserts (left) and the twenty pair Differential Pair inserts (right). Backplane inserts are at the top of the photograph, module inserts at the bottom.

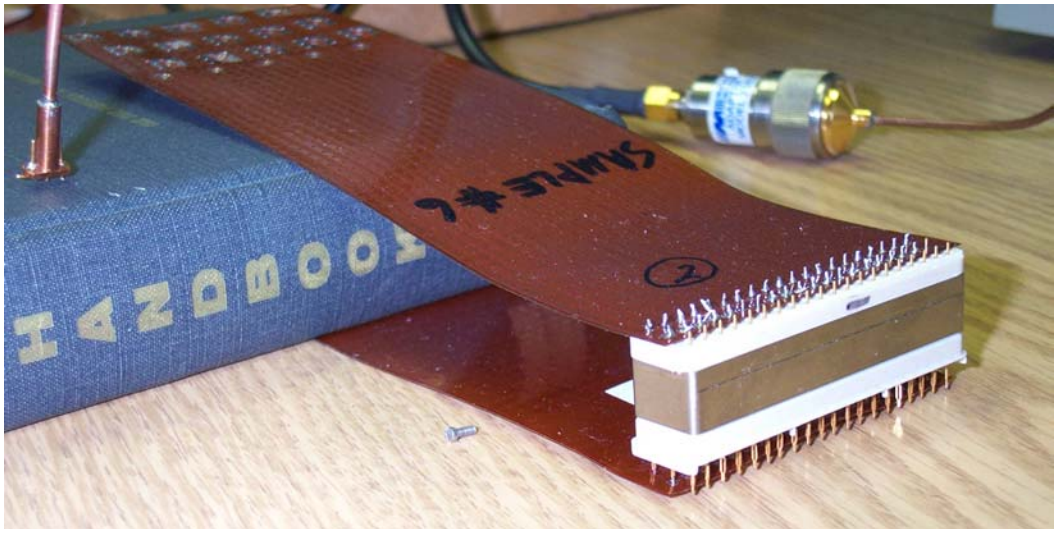


Figure 7. Electrical Characterization Test Samples, mated and attached to Flex Print.

Testing was done using a Tektronix differential TDR. Measured results are shown below. Figures 8, 9, and 10 show the differential pair impedance at 35, 150, and 300 picosecond input risetimes, respectively.

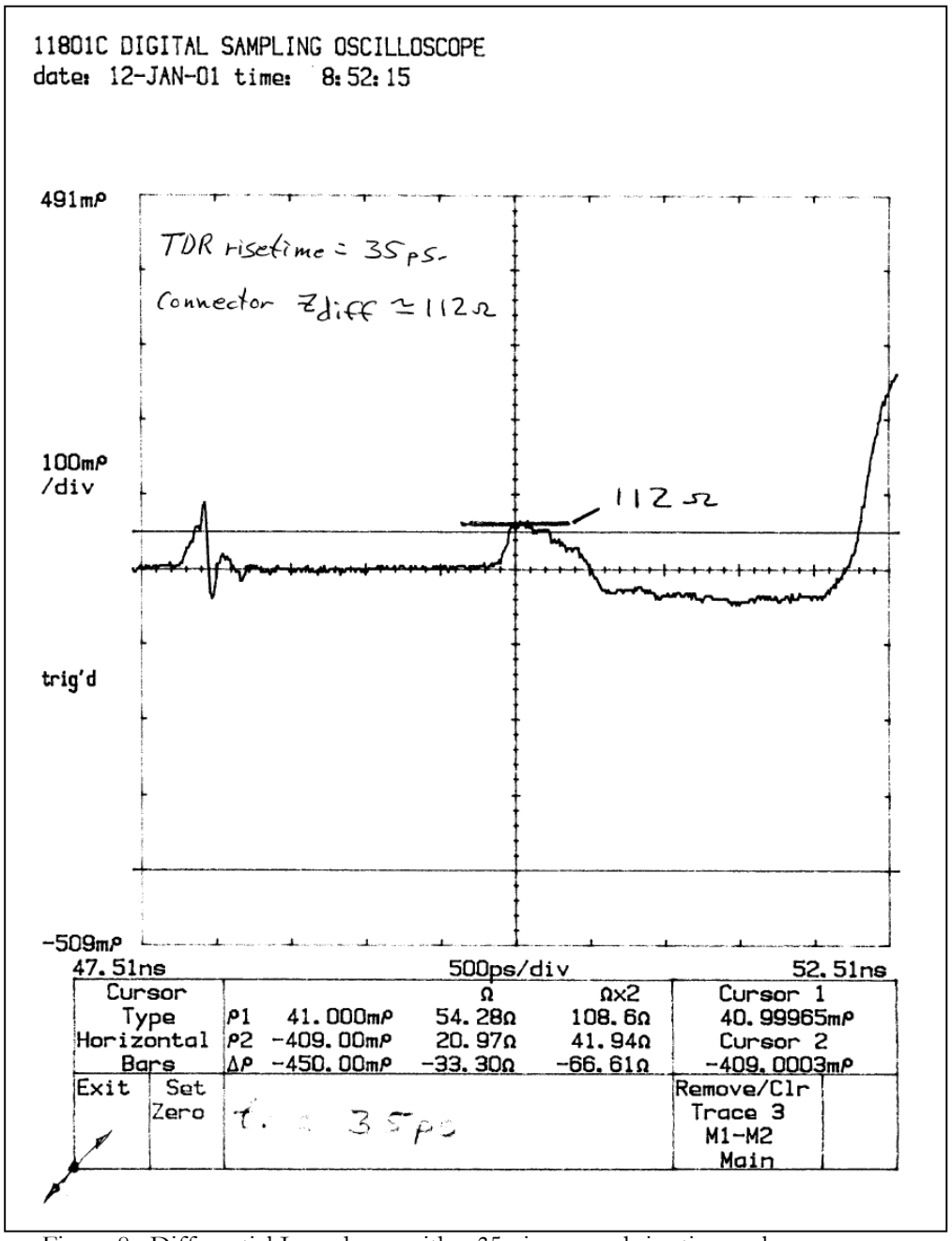


Figure 8. Differential Impedance with a 35 picosecond rise time pulse.

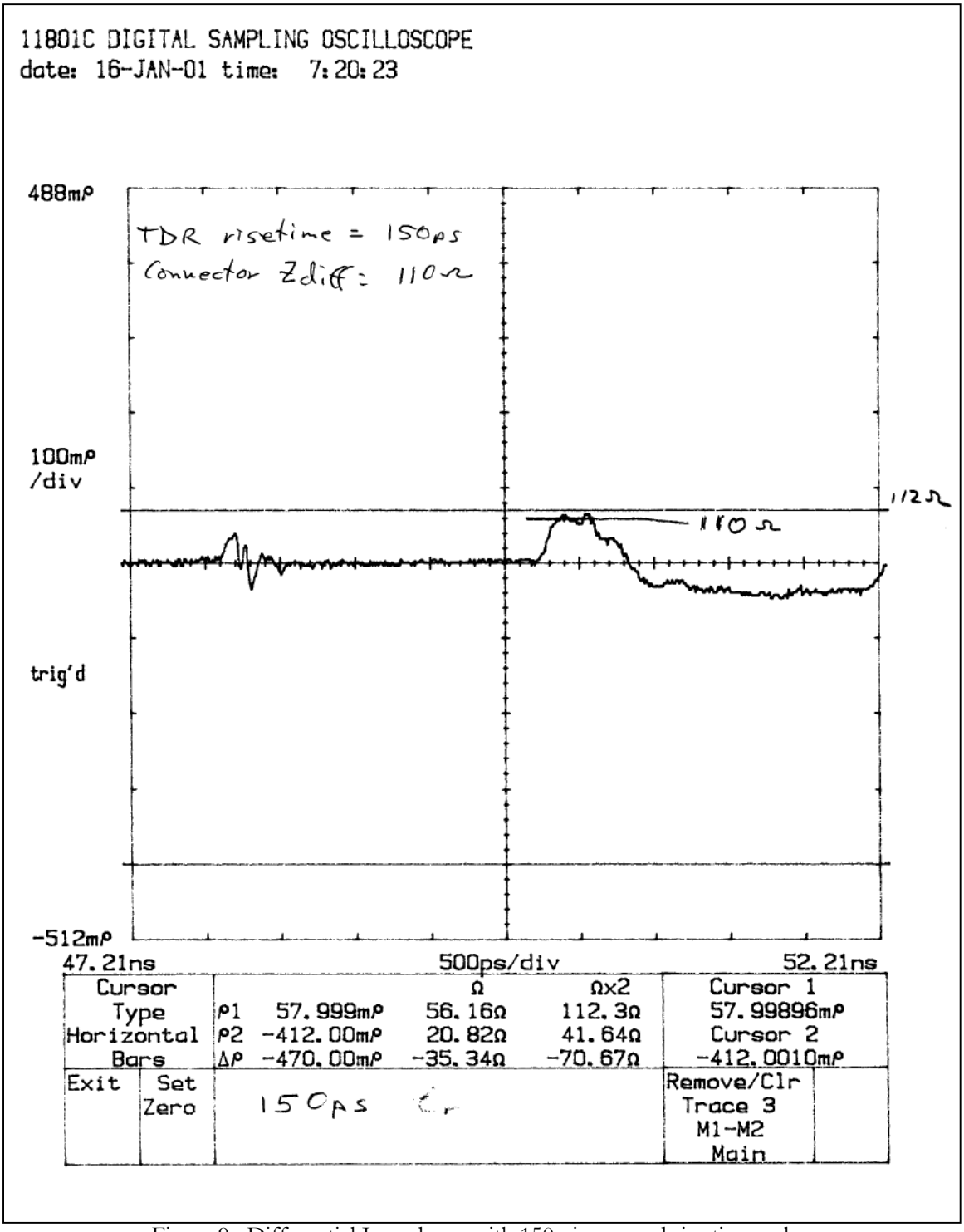


Figure 9. Differential Impedance with 150 picosecond rise time pulse.

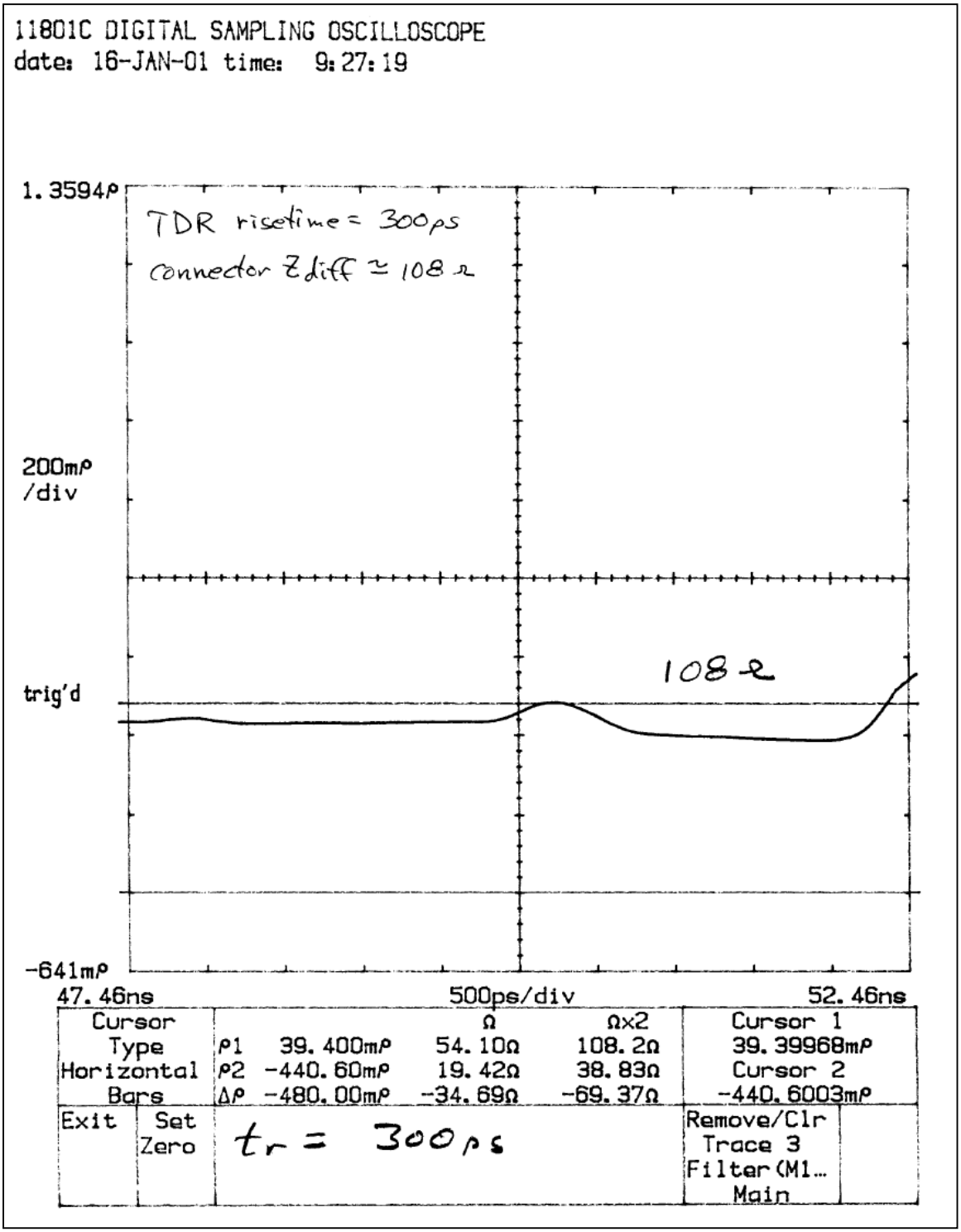


Figure 10. Differential Impedance with a 300 picosecond risetime pulse.

Figures 11 through 14 show crosstalk at 35 ps risetime for the quiet line with both open circuit and 50 ohm terminations.

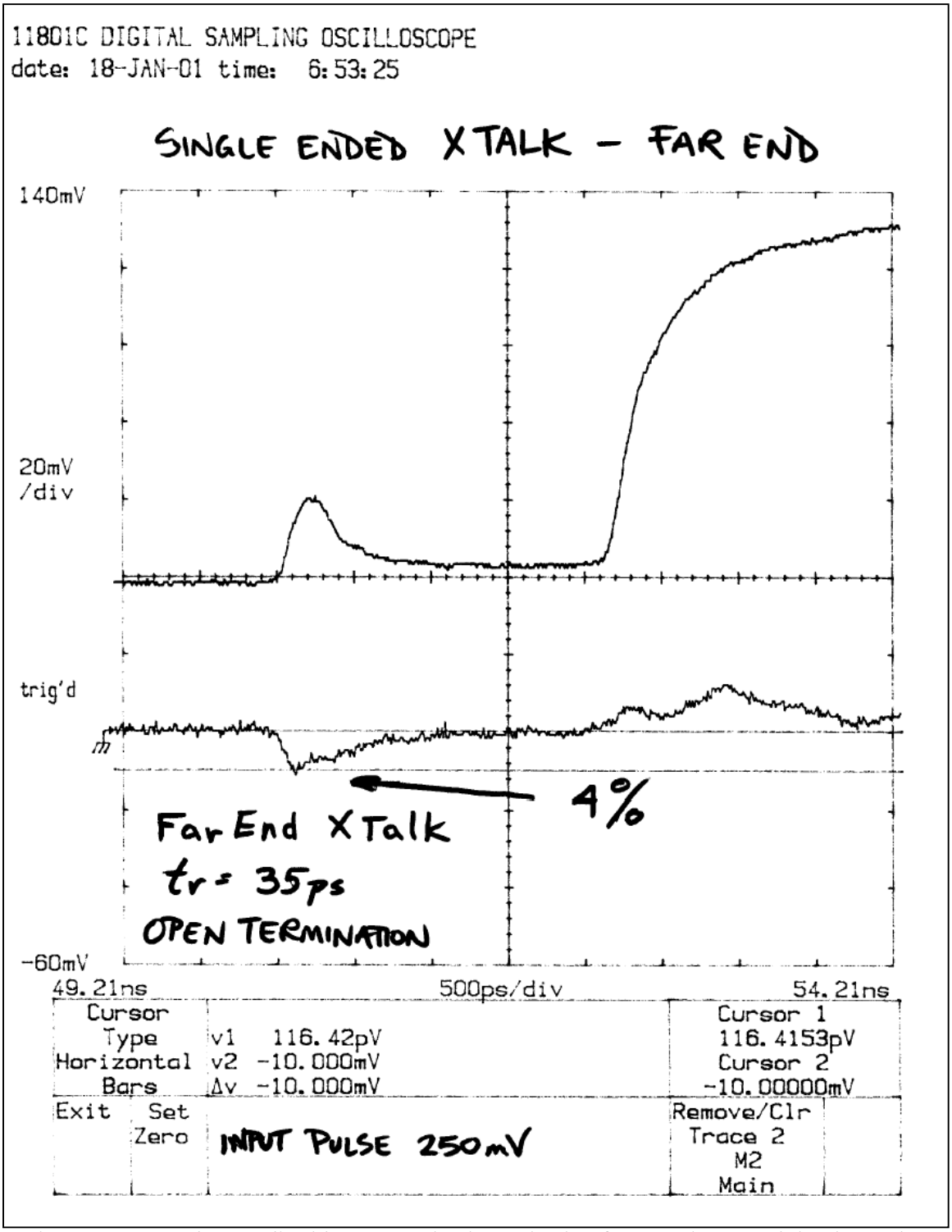


Figure 11. Far end crosstalk with an open circuit termination for a 35 picosecond rise time pulse.

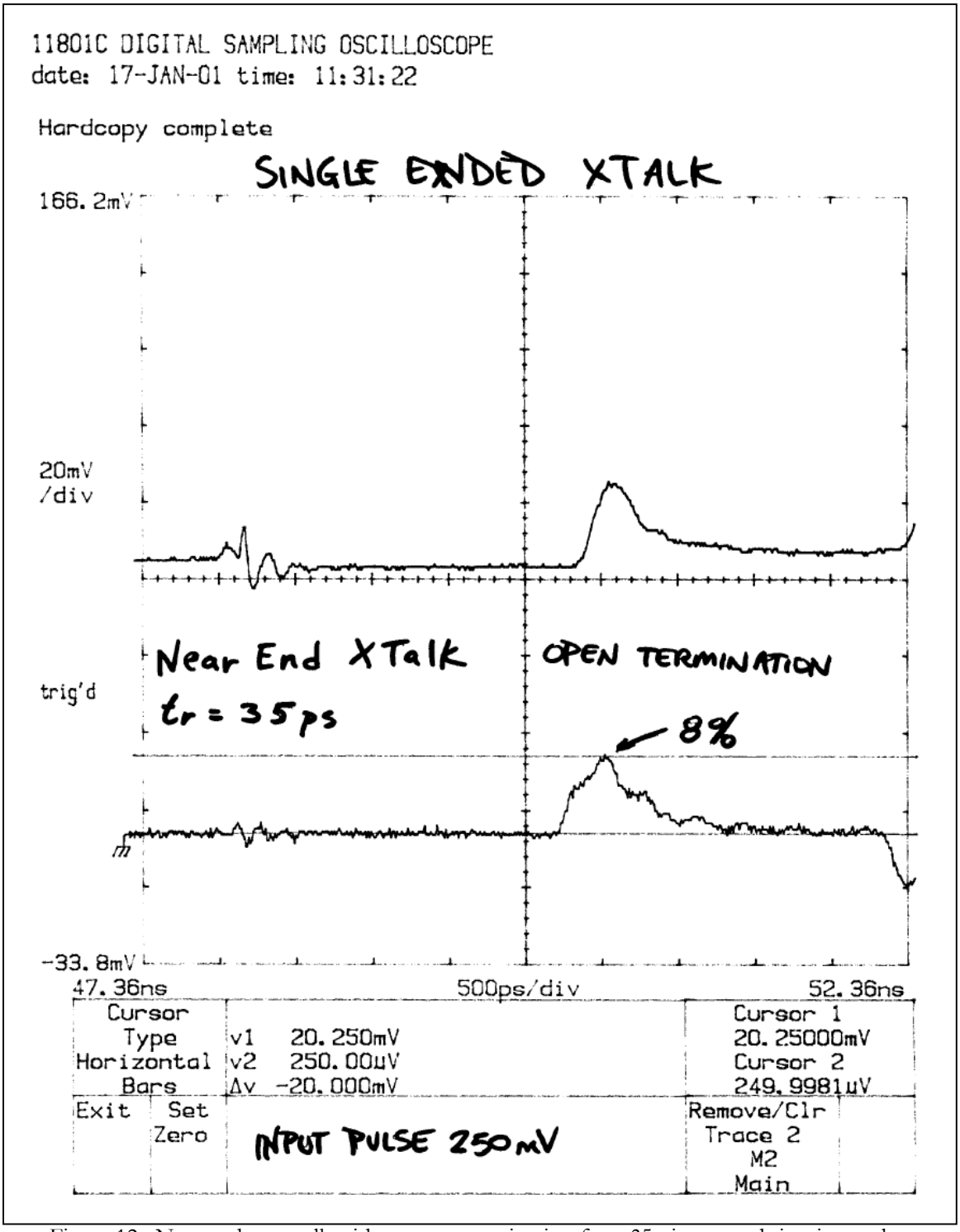


Figure 12. Near end crosstalk with an open termination for a 35 picosecond rise time pulse.

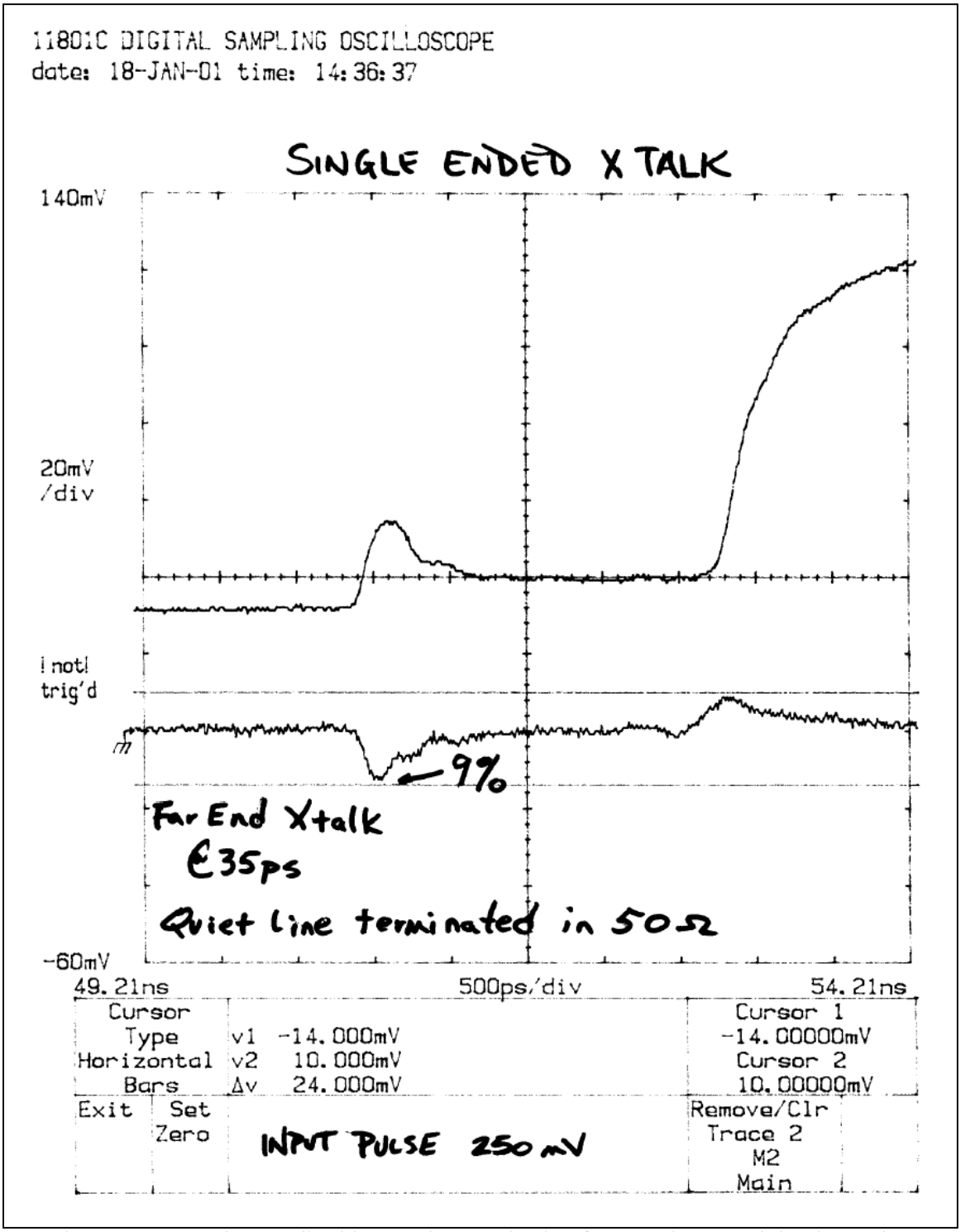


Figure 13. Far end crosstalk with a 50 ohm termination for a 35 picosecond rise time pulse.

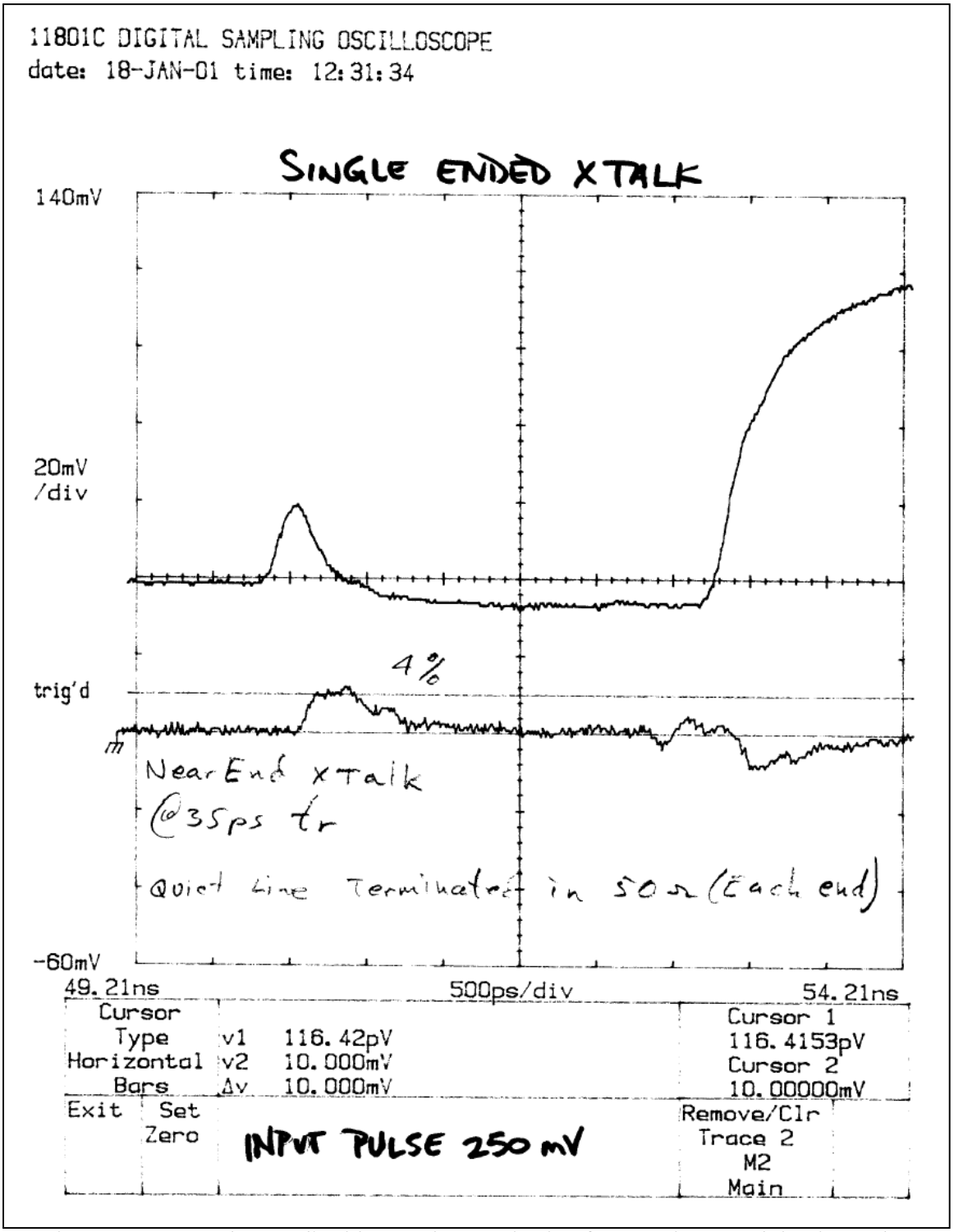


Figure 14. Near end crosstalk with a 50 ohm termination for a 35 picosecond rise time pulse.

CONCLUSIONS AND RECOMMENDATIONS

Characteristic Impedance:

The measured differential characteristic impedance of 108 to 112 ohms is higher than the modeled 100 ohms. This is probably due (at least in part) to a 1/8 inch air gap between the test flex board and back side of the mother board connector. (visible in Figure 3) This condition occurred because the compliant pins on the backplane connector insert are slightly larger in diameter than the through holes in the flex print, thus not allowing full insertion. The 1/8 inch of exposed pin is highly inductive, raising the impedance at that point to around 180 to 200 ohms. (differential, modeled) In normal usage, this condition would not occur.

Discounting any effects of the fixturing gap, a slightly higher than predicted differential impedance will tend to offset any capacitive discontinuities introduced by module and backplane termination pads.

Crosstalk:

The measured crosstalk at 35 picosecond input risetime was in fairly good agreement with simulated results. (9 % measured vs. 9.7 % simulated) Measurements at slower (more realistic) risetimes were not performed. It is expected that measured results would be in good agreement with predicted values.

Recommendations for further work:

Additional testing to be performed should include crosstalk measurements at various risetimes, and imepdance measurements with modified fixturing that removes the inductive gap mentioned earlier. It is expected that the 108-112 ohm measured differential impedance will still be in the 104-105 ohm range after the fixturing gap is removed.

ADDENDUM 1 - EYE PATTERN SIMULATIONS

The SPICE model used for this report was also used to generate eye diagrams for various combinations of connector(s), printed circuit board via capacitances, and data rates.

The input waveform for each simulation was a psuedo random bit stream produced by a simple BASIC program taken from Microsim application notes. The edge rate used for the four data rates simulated (1, 2, 5, and 10 Gigabits per second) was 60 picoseconds.

Simulations were run for a single mated pair of connectors (plots 1-4). Knowing that the transition from the connector to the printed circuit board will contain capacitive discontinuities due to pads and vias, additional simulations (plots 5-8) were run with 1.5 pF elements at both the input and output of the SPICE model of the mated pair of connectors.

Simulations were also conducted for 2 mated pairs of connectors, separated by 18 inches of lossless transmission line (plots 9-12 without vias, plots 13-16 with vias). This was done to simulate module to module communication through two connectors and a backplane.

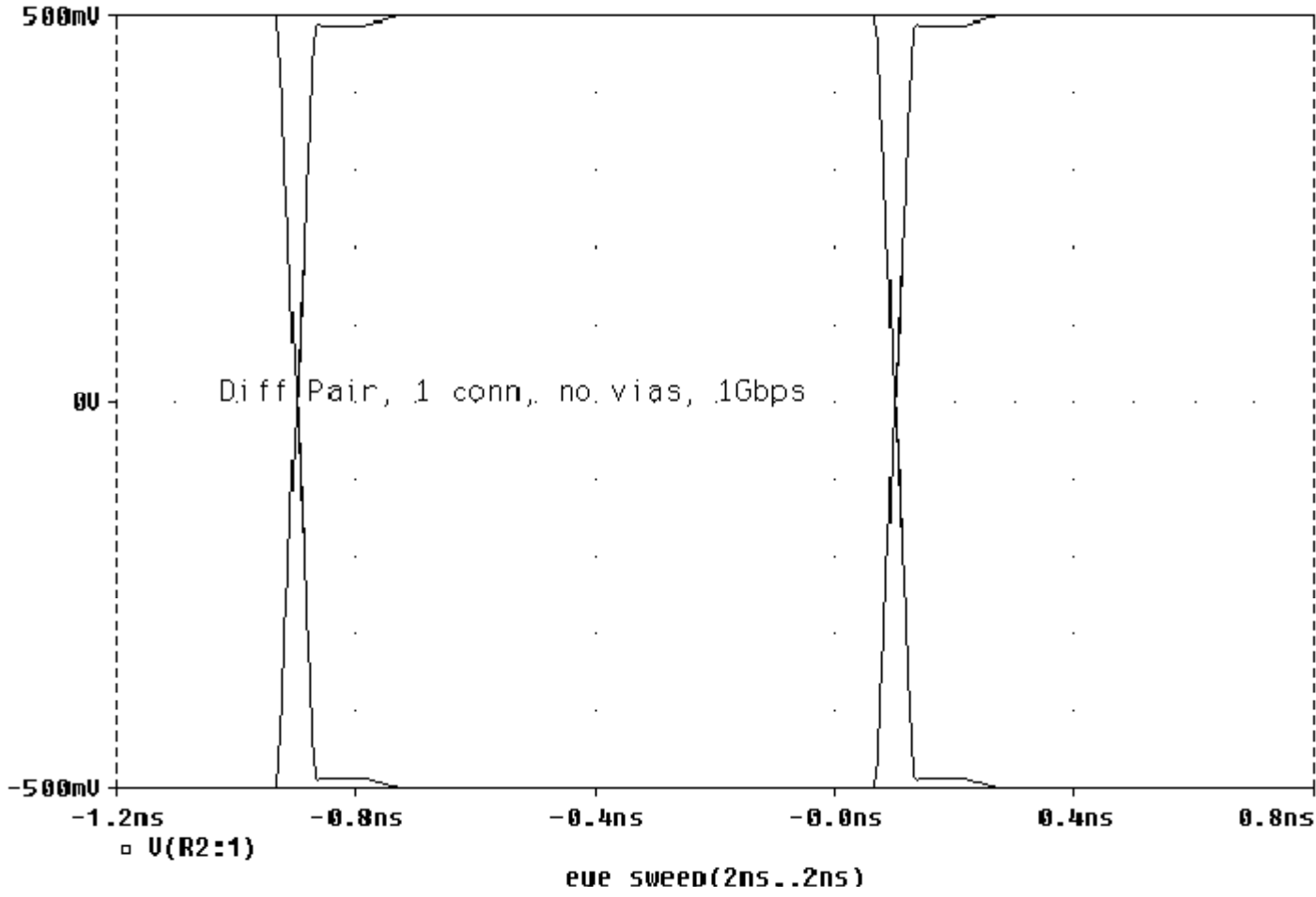
EYE DIAGRAM SIMULATION CONCLUSIONS

Simulation has shown that the Amphenol Staggered Grid LRM 100 Ohm Differential Pair connectors by themselves were capable of transmitting 10 Gbps, assuming a perfect transition between the connectors and the printed circuit boards, and loss-less transmission lines in the printed circuit boards. Knowing parasitic capacitance will undoubtedly occur at the transitions, simulation indicates that the connector was capable of conducting data rates of at least 2 Gbps (with 1.5 pF capacitance at the transitions). In order to maximize the data rate capacity of any connector, users must minimize parasitic capacitance at the transition between the connector and the printed circuit boards.

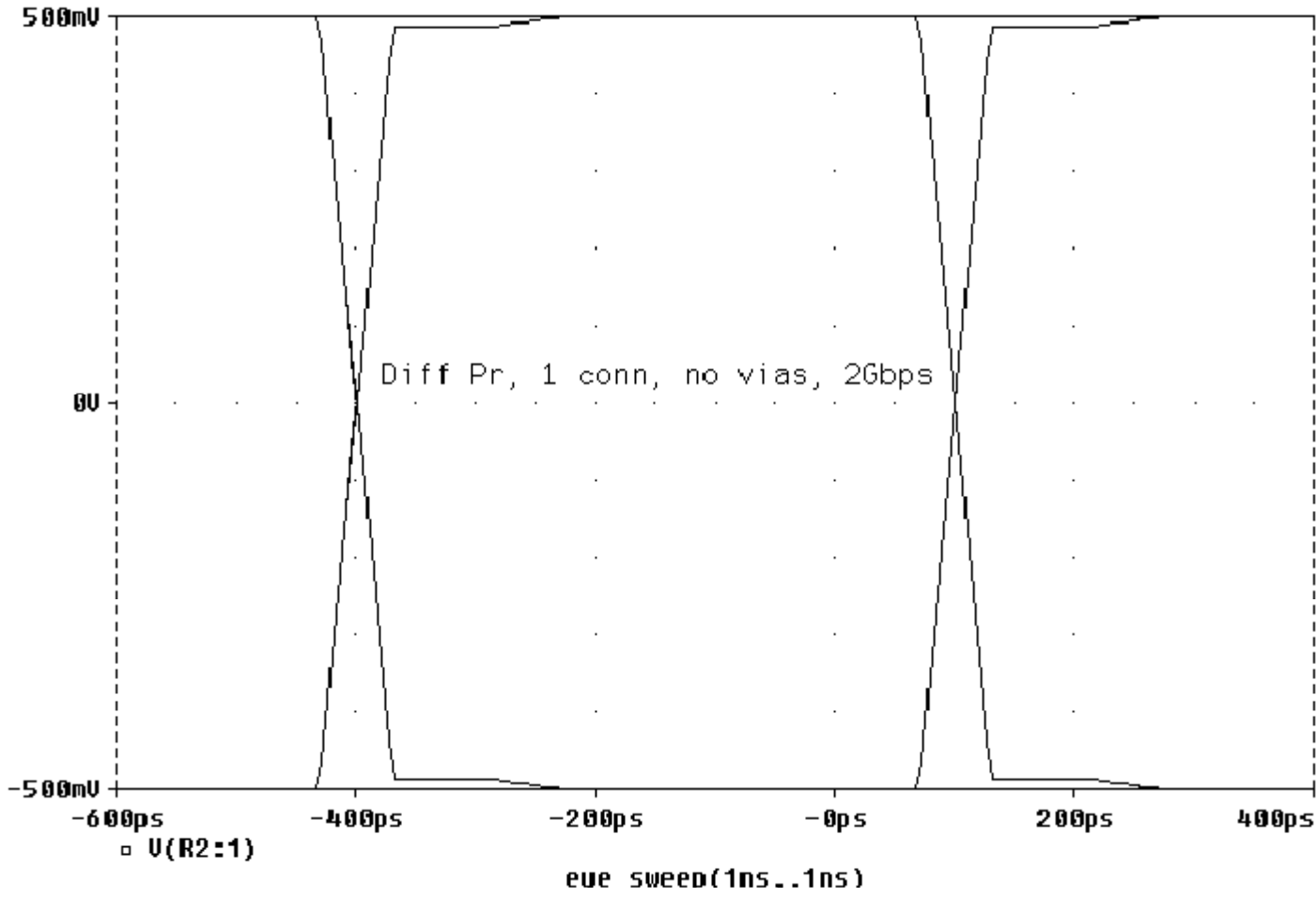
Additional degradation due to "real" (lossy) board traces was not taken into consideration for this simulation effort. Industry literature confirms that the parasitic capacitance of a typical via is one of the major limitations to operating at 5 Gbps and beyond, assuming properly designed, impedance matched connectors and printed circuit boards.

Recommendations for further work:

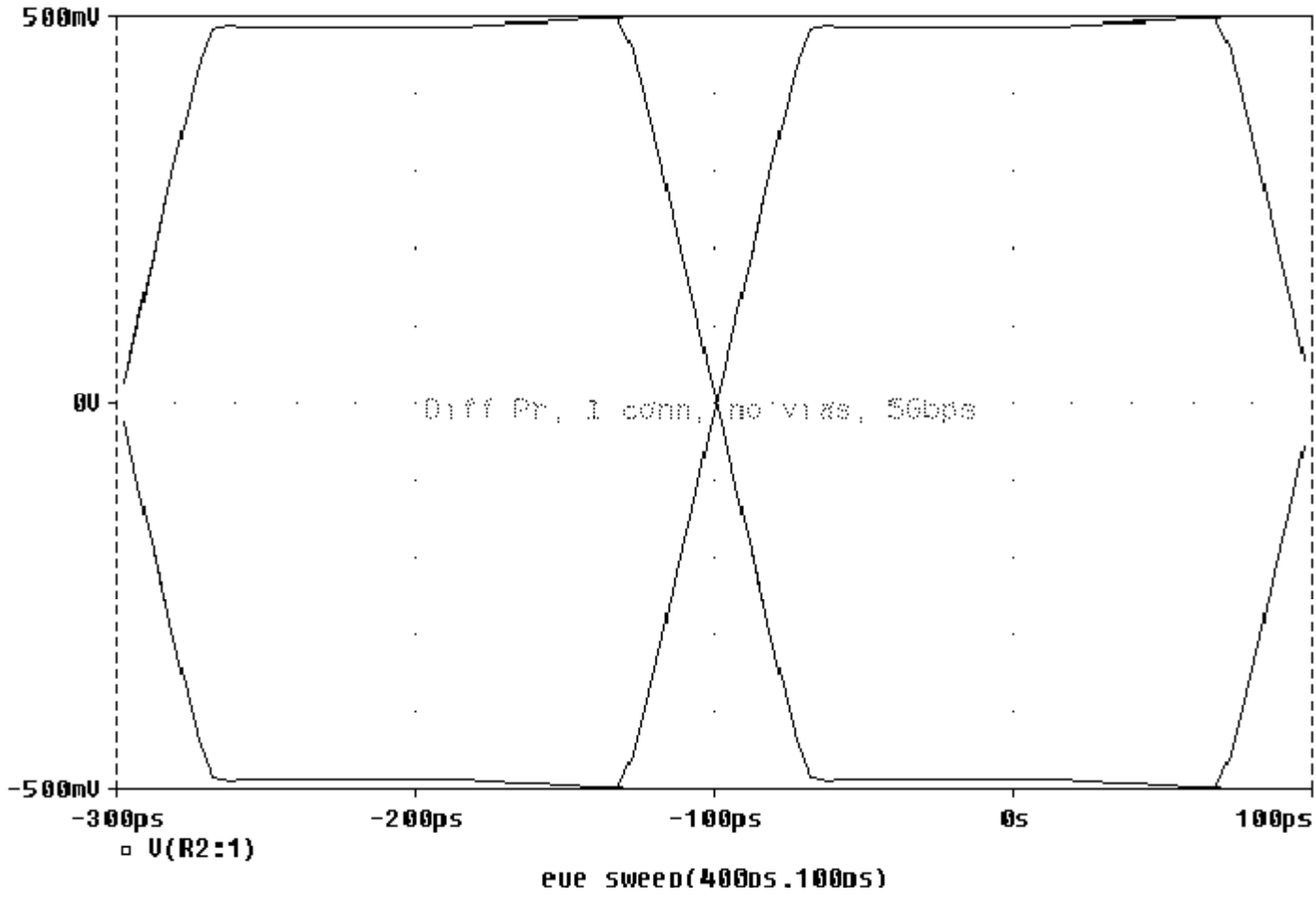
Testing should be conducted to verify eye diagram performance (in accordance with EIA-364-107 or equivalent test specification).



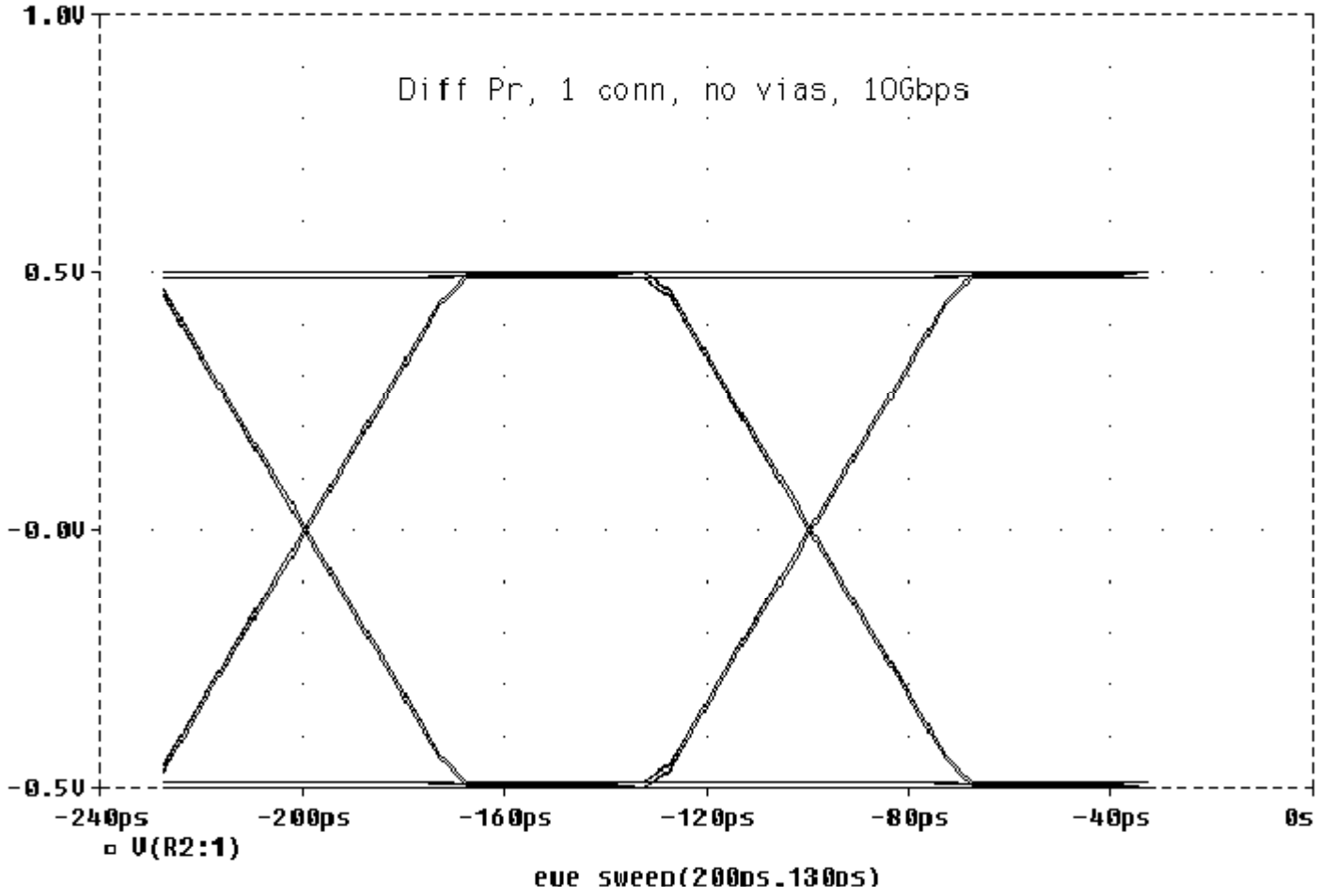
Plot 1: Single Connector Pair, No Vias, 1 Gbps



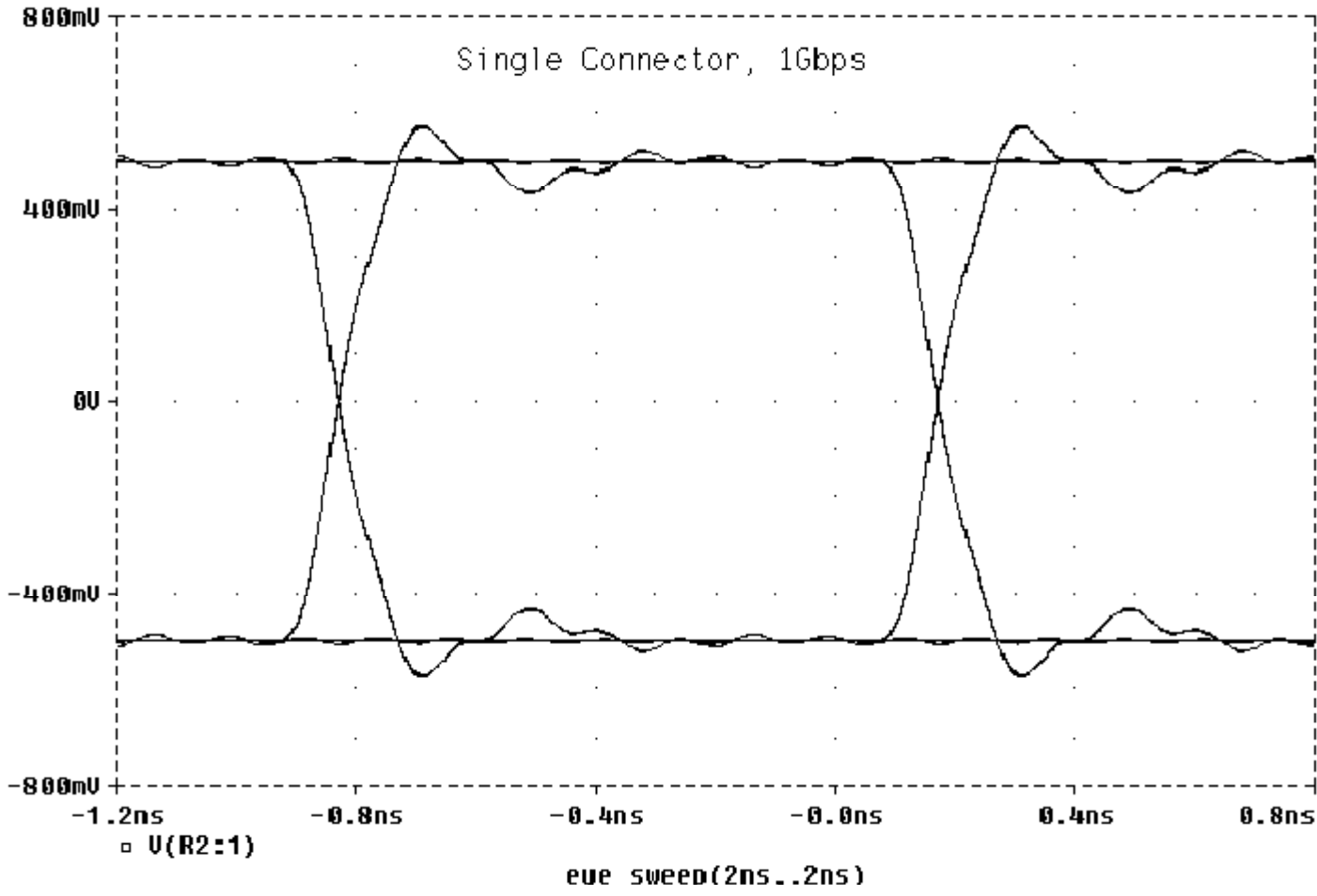
Plot 2: Single Connector Pair, No Vias, 2 Gbps



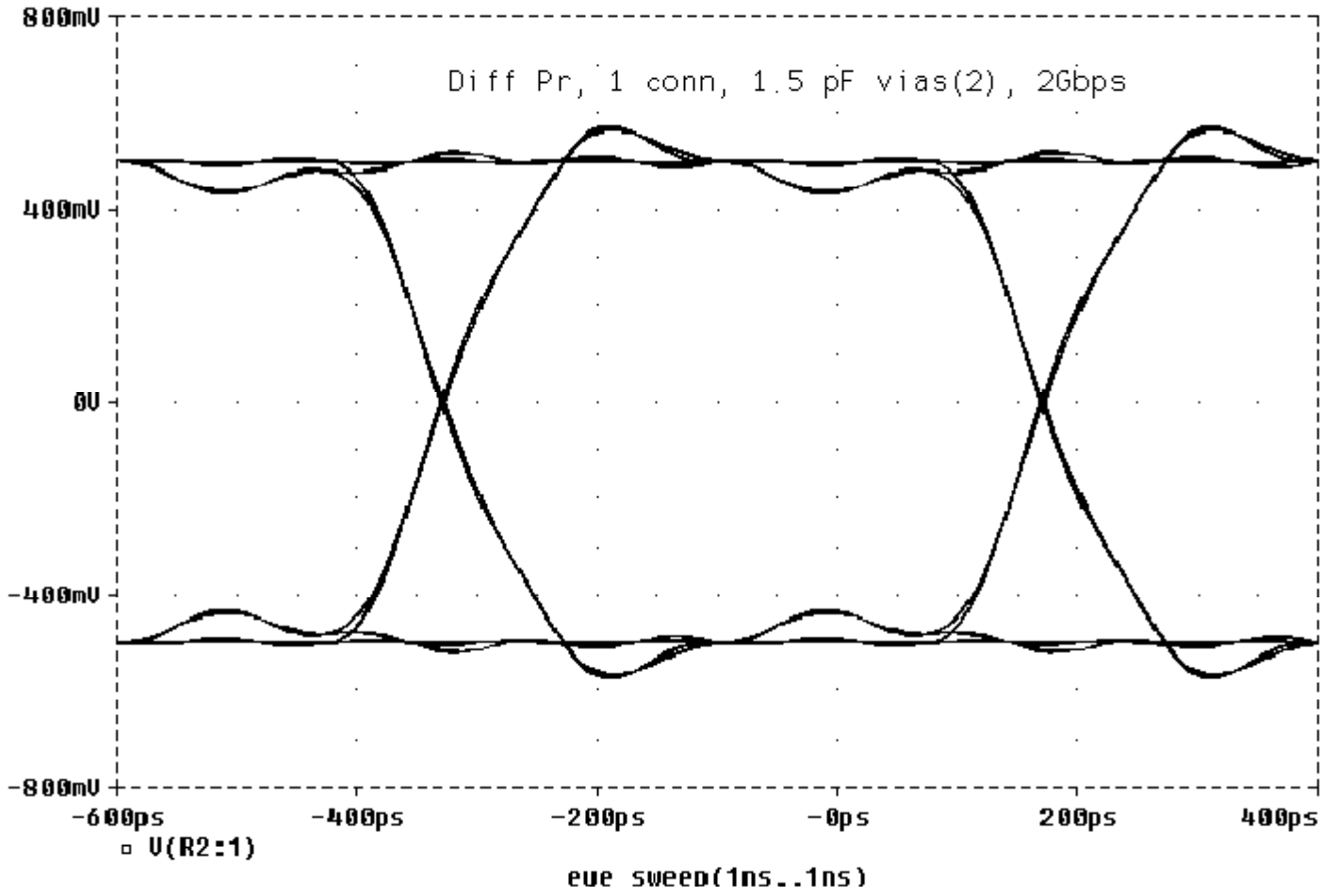
Plot 3: Single Connector Pair, No Vias, 5 Gbps



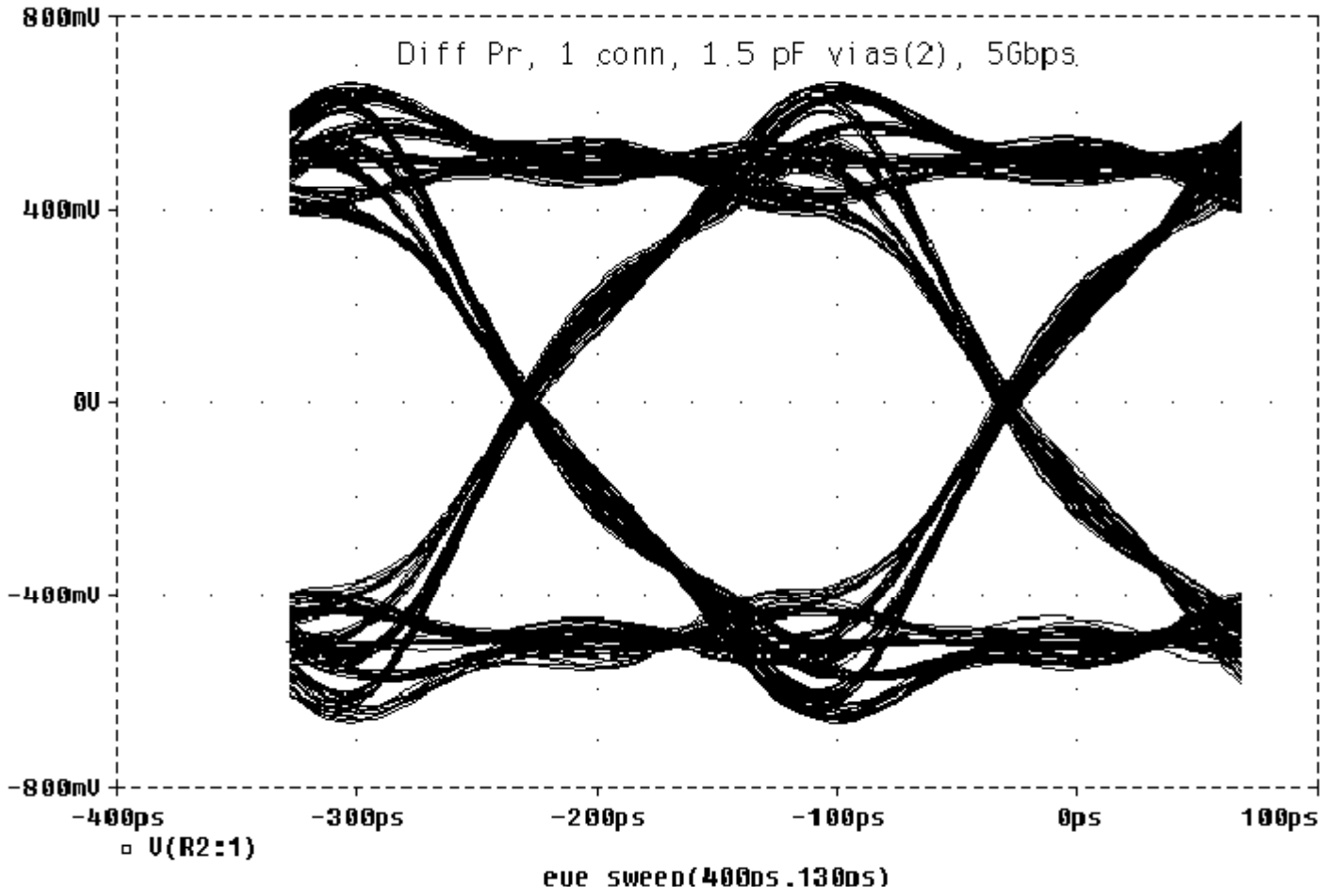
Plot 4: Single Connector Pair, No Vias, 10 Gbps



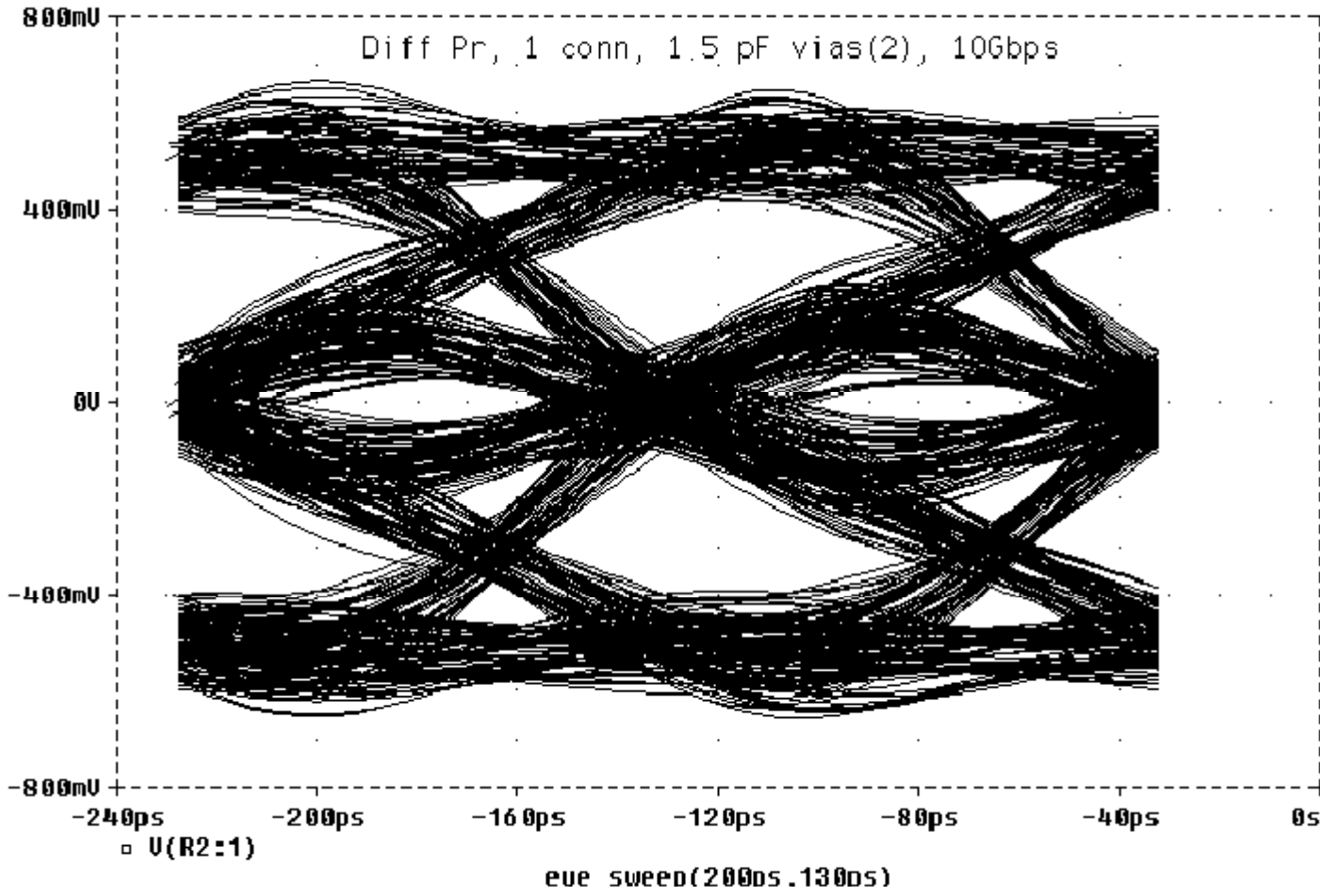
Plot 5: Single Connector Pair, With 1.5 pF Vias, 1 Gbps



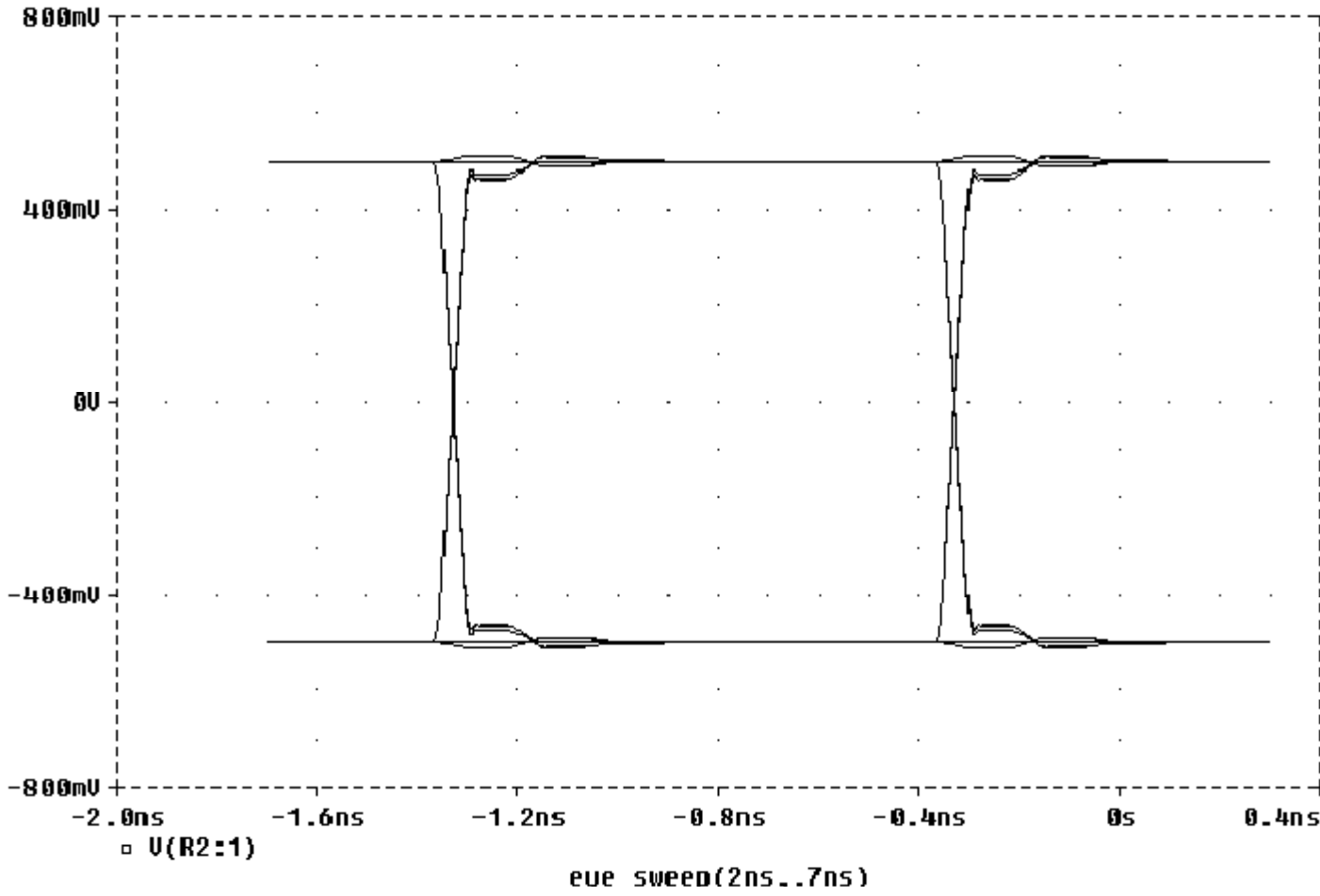
Plot 6: Single Connector Pair, With 1.5 pF Vias, 2 Gbps



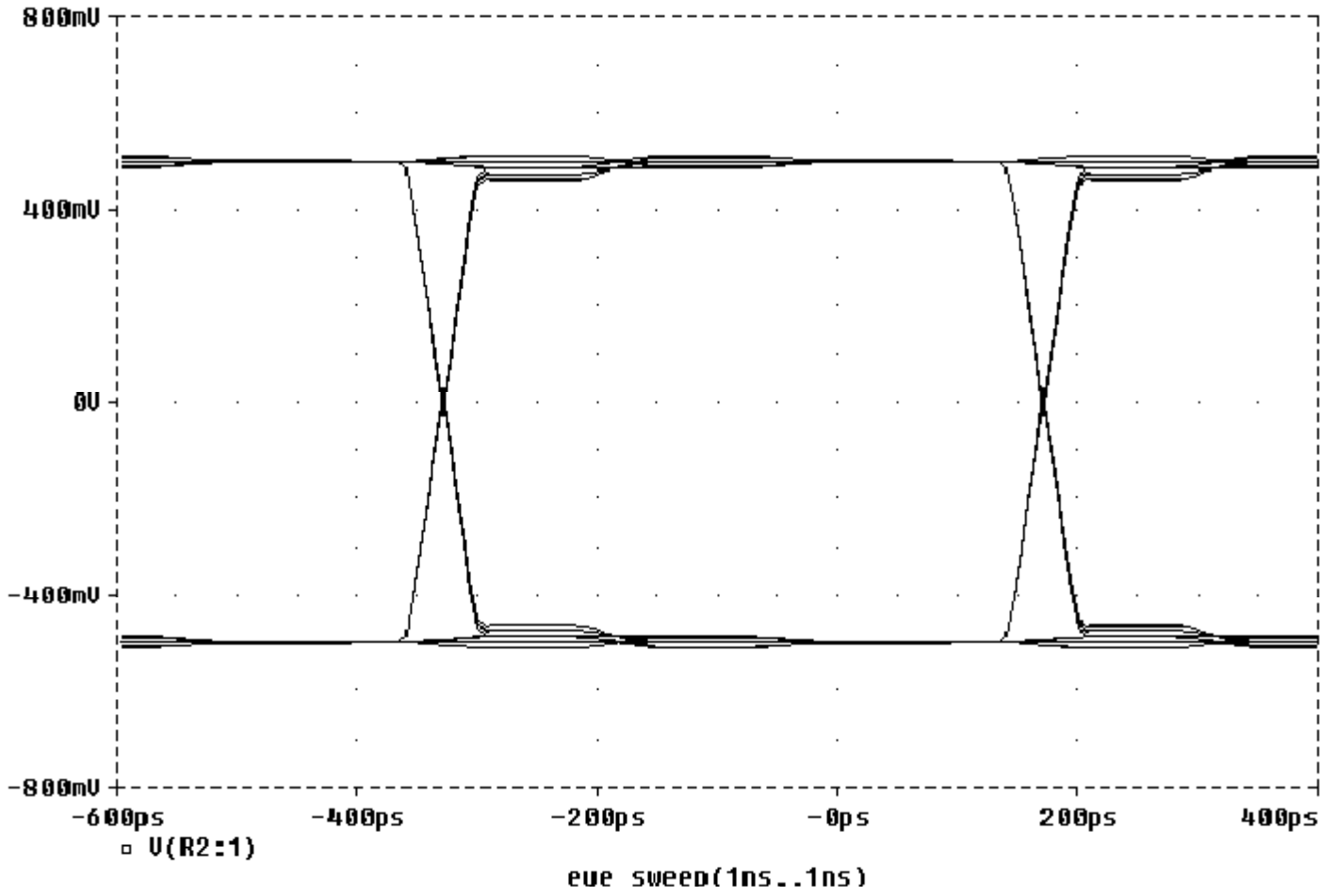
Plot 7: Single Connector Pair, With 1.5 pF Vias, 5 Gbps



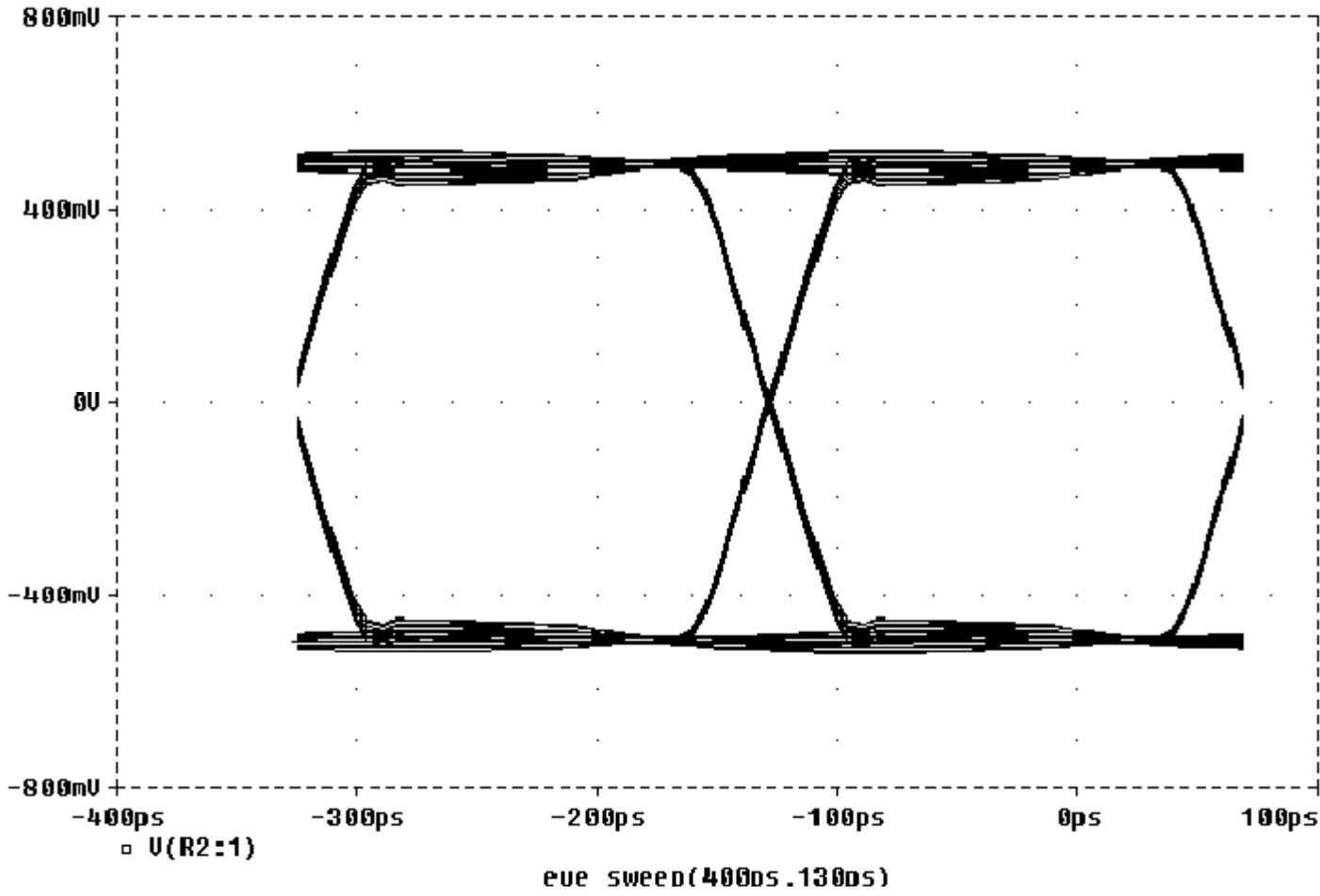
Plot 8: Single Connector Pair, With 1.5 pF Vias, 10 Gbps



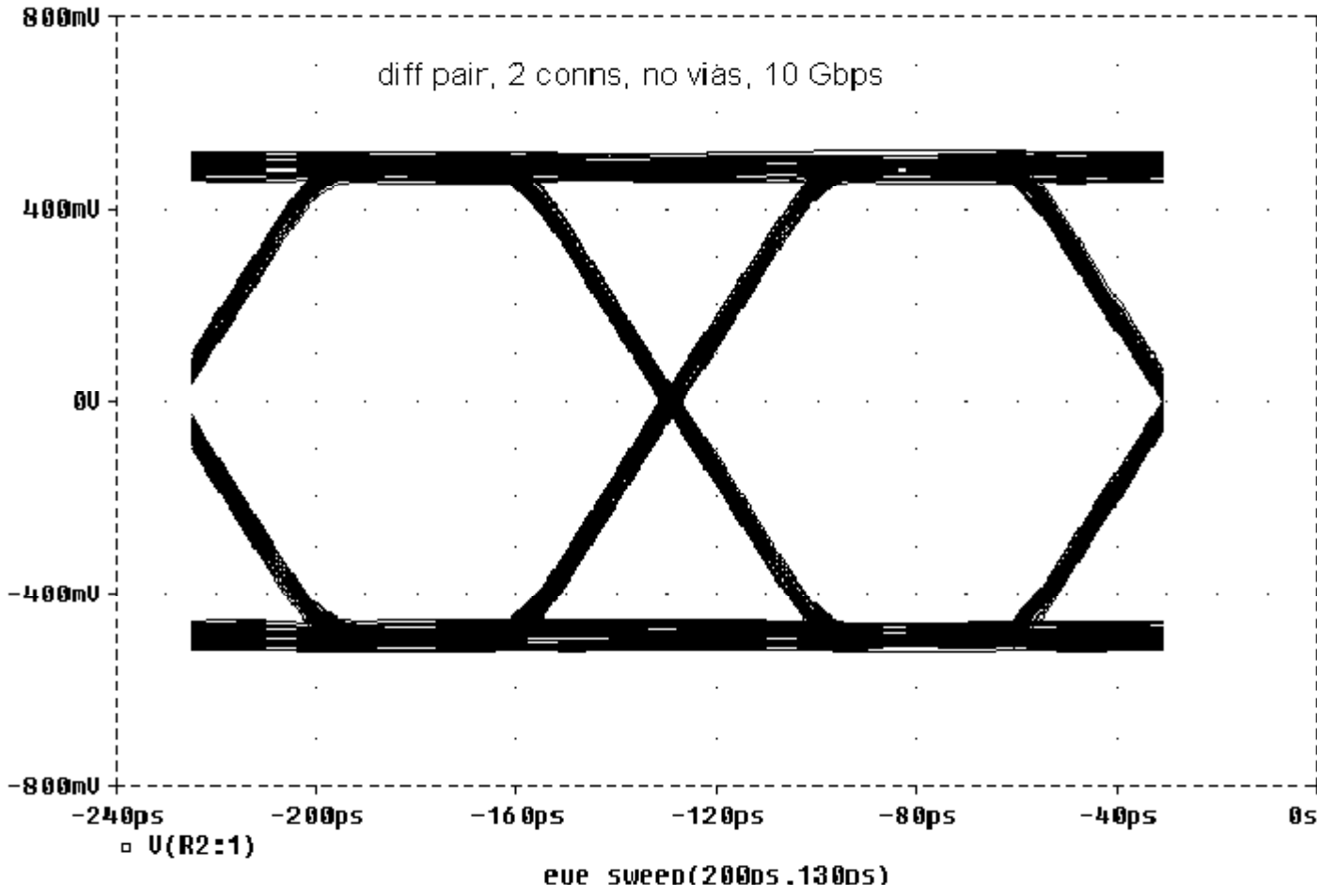
Plot 9: Two Connector Pairs, No Vias, 1 Gbps



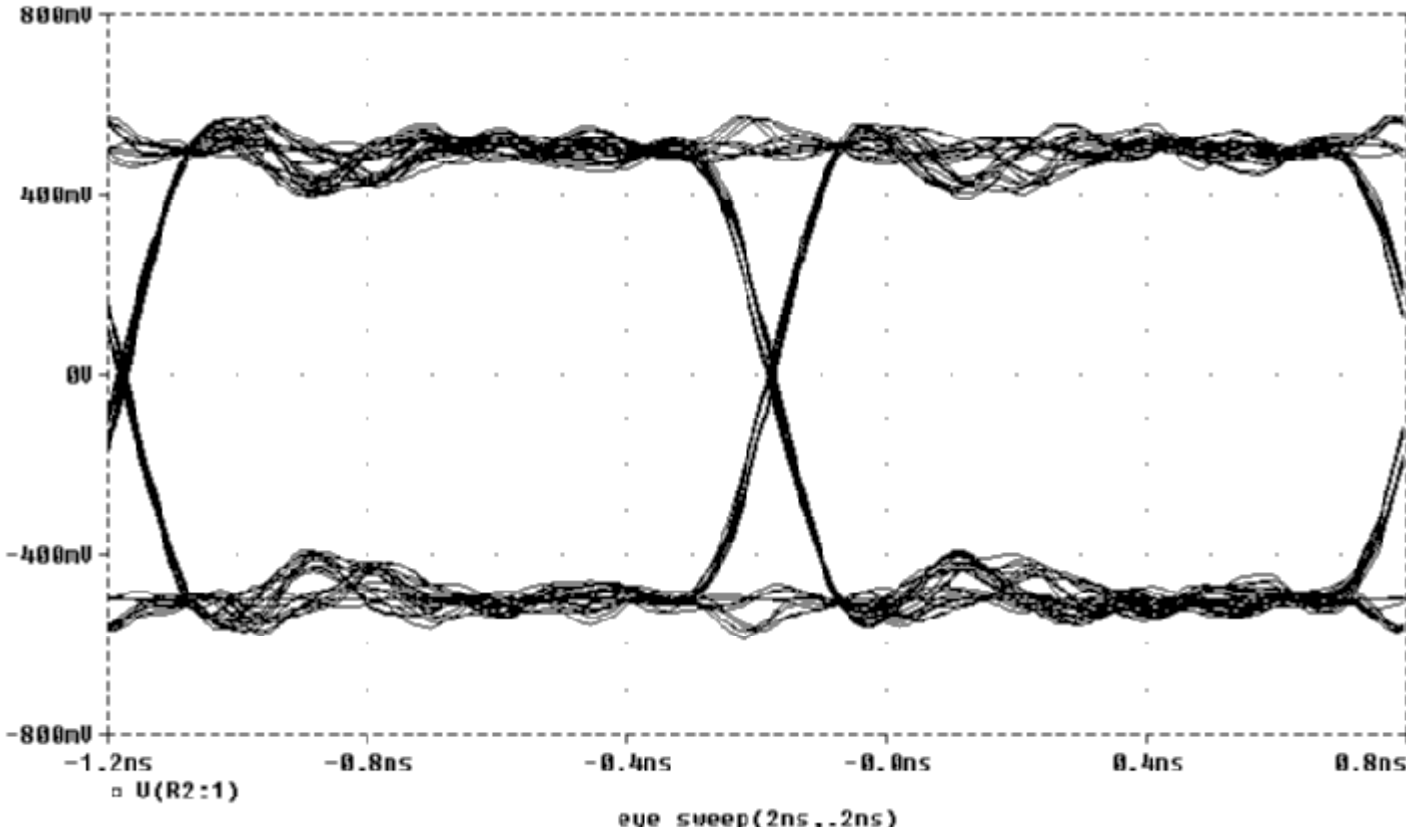
Plot 10: Two Connector Pairs, No Vias, 2 Gbps



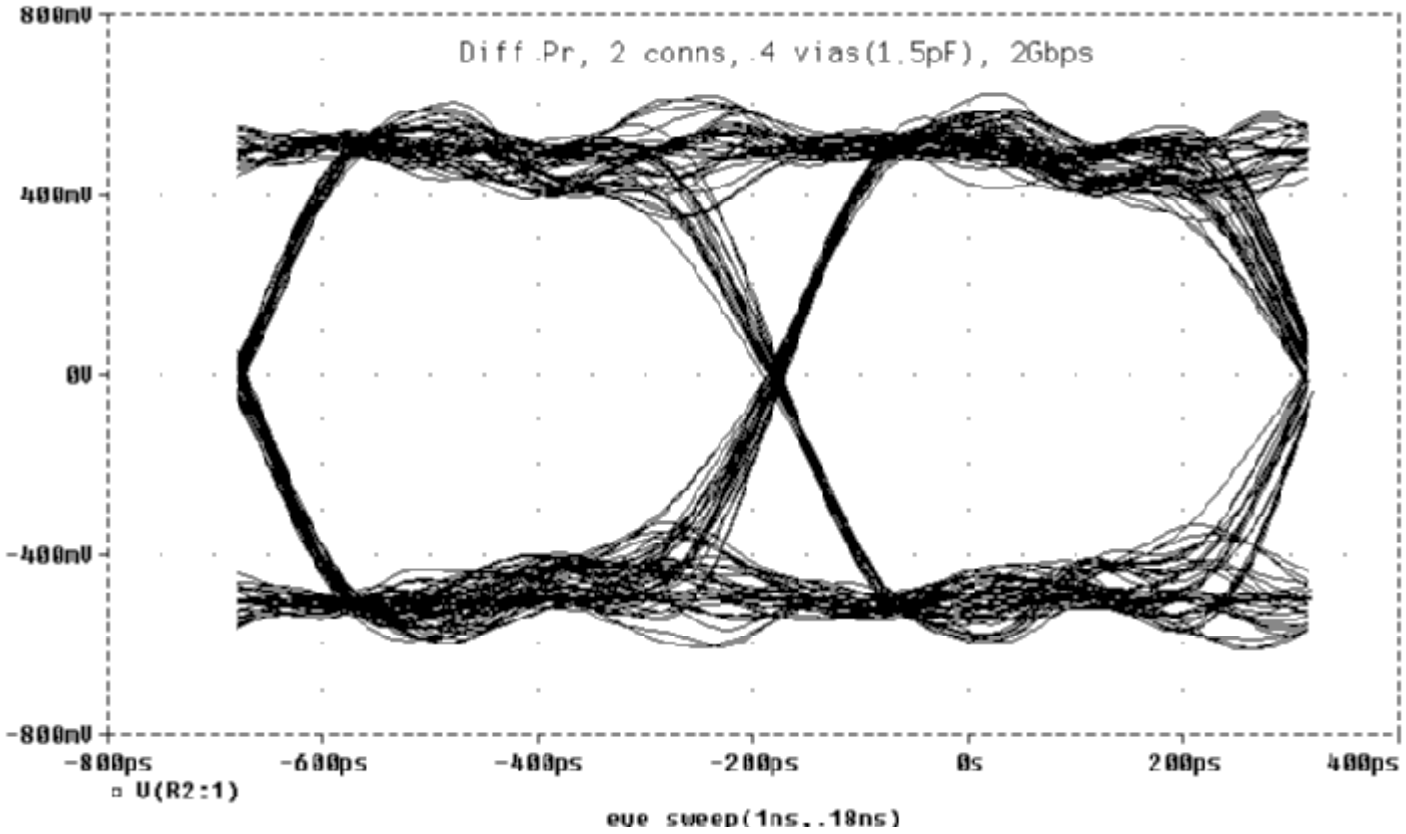
Plot 11: Two Connector Pairs, No Vias, 5 Gbps



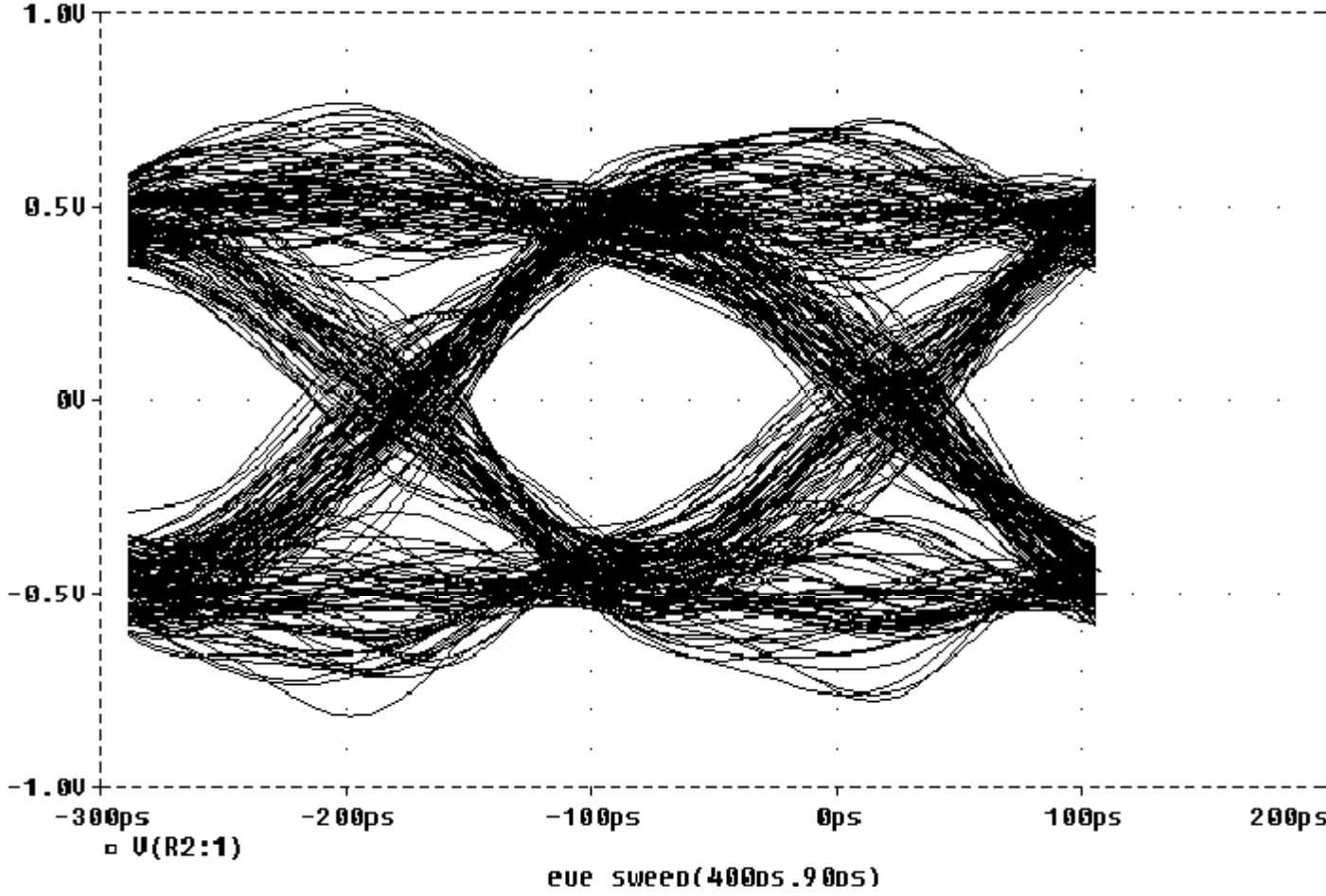
Plot 12: Two Connector Pairs, No Vias, 10 Gbps



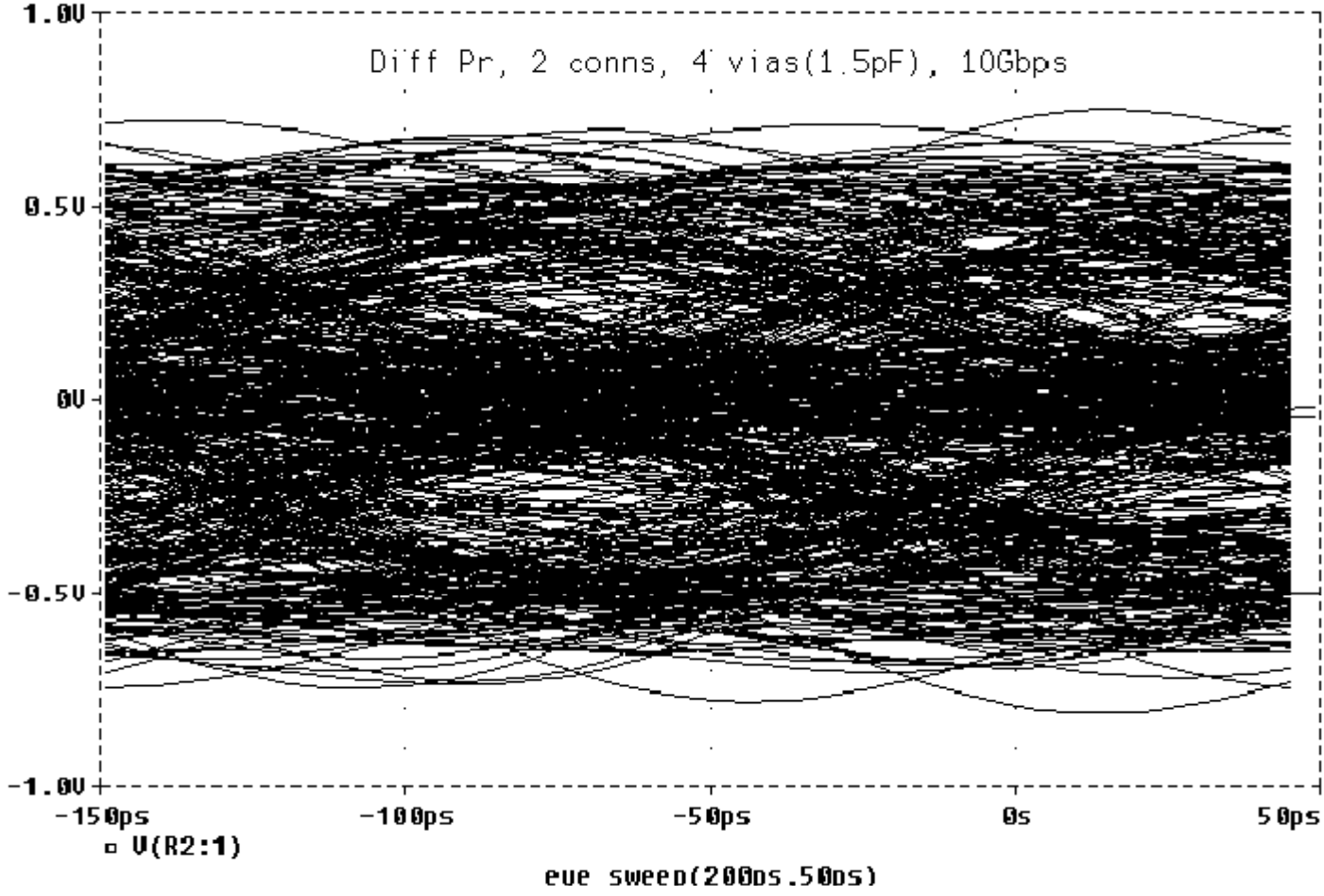
Plot 13: Two Connector Pairs, With Vias, 1 Gbps



Plot 14: Two Connector Pairs, With Vias, 2 Gbps



Plot 15: Two Connector Pairs, With Vias, 5 Gbps



Plot 16: Two Connector Pairs, With Vias, 10 Gbps