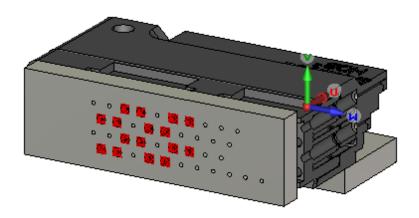
HSB3 Signal Integrity Analysis

All Rows, De-populated (No Grounds)



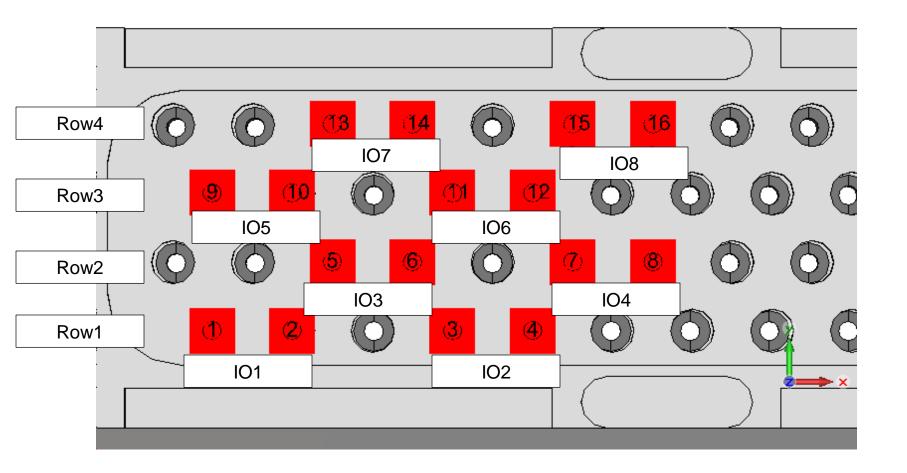
HSB3 (No Grounds) CST 3D Model





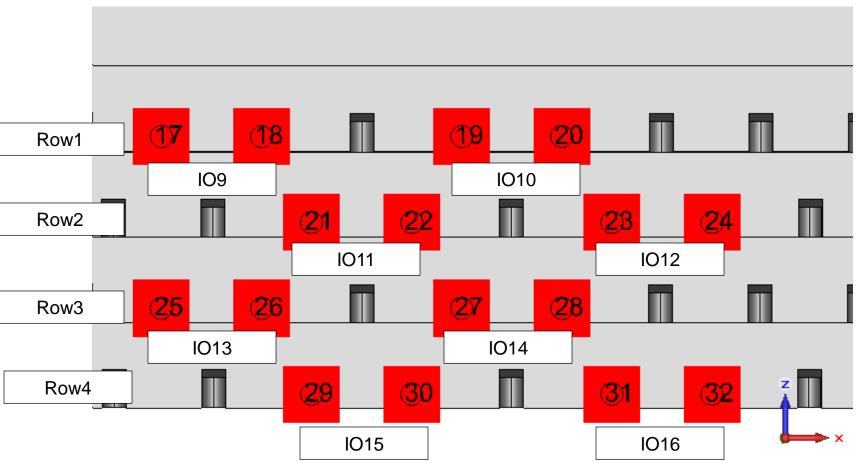
Backplane Port Numbering

(IO1 thru 7 are corresponding mixed mode ports on Test Bed and Channel simulation schematics)



Daughter Card Port Numbering

(IO9 thru 16 are corresponding mixed mode ports on Test Bed and Channel simulation schematics)

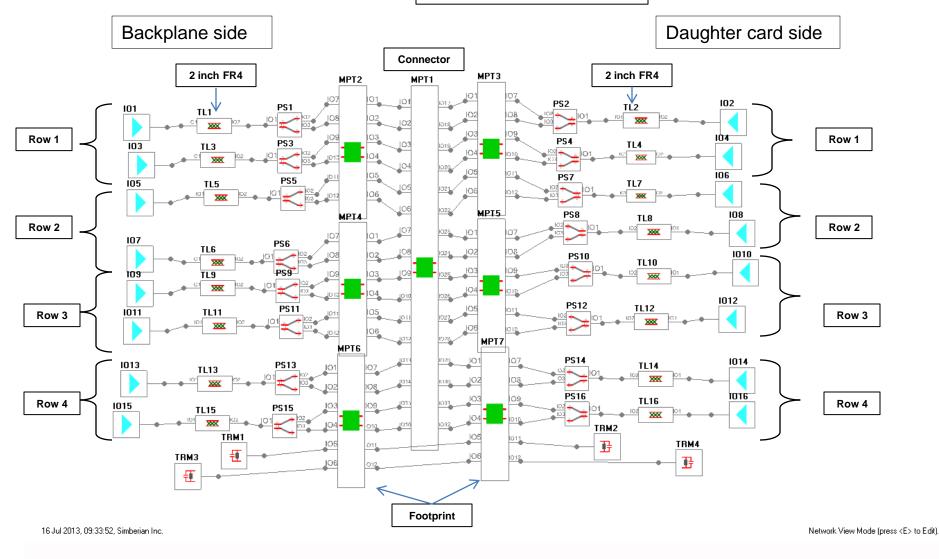


Test Bed Simulation Schematic

PS 1 thru 32 are single ended to differential convertors.

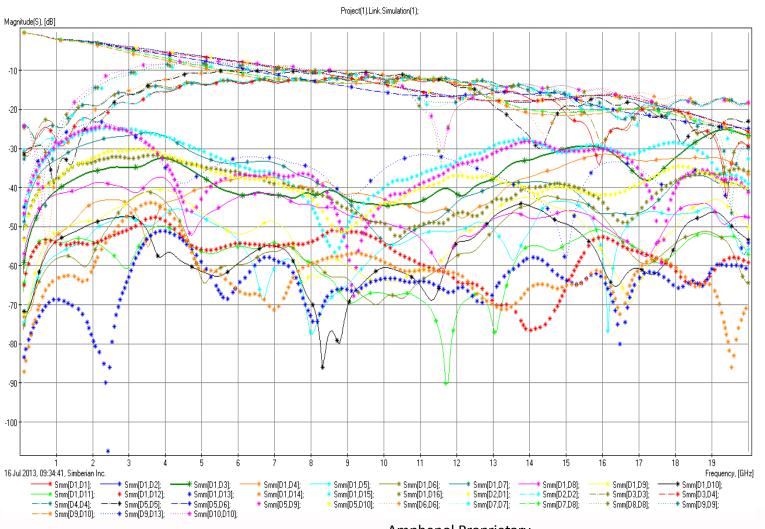
IO1 thru 16 are Mixed Mode ports.

TRM1 thru 4 are ideal 50 ohm terminations for unused footprint ports.

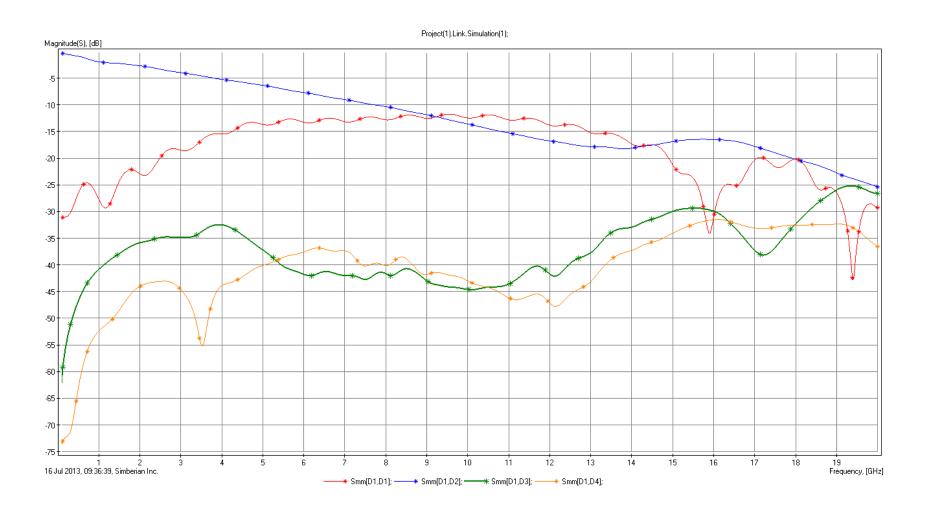


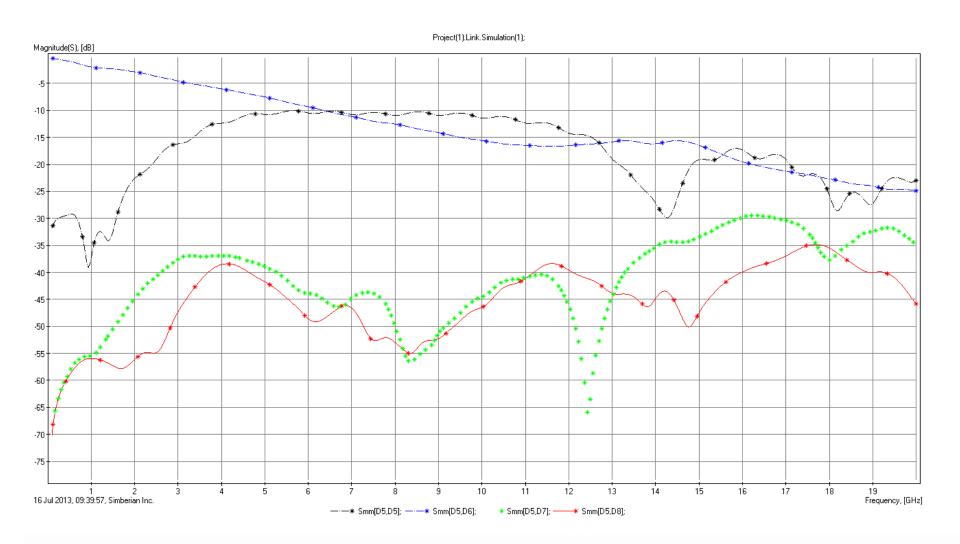


General S Parameters

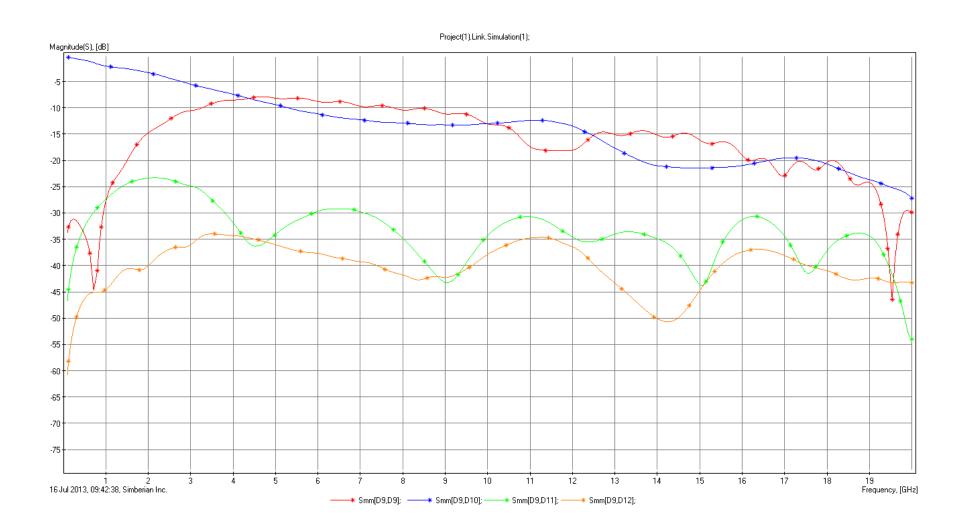




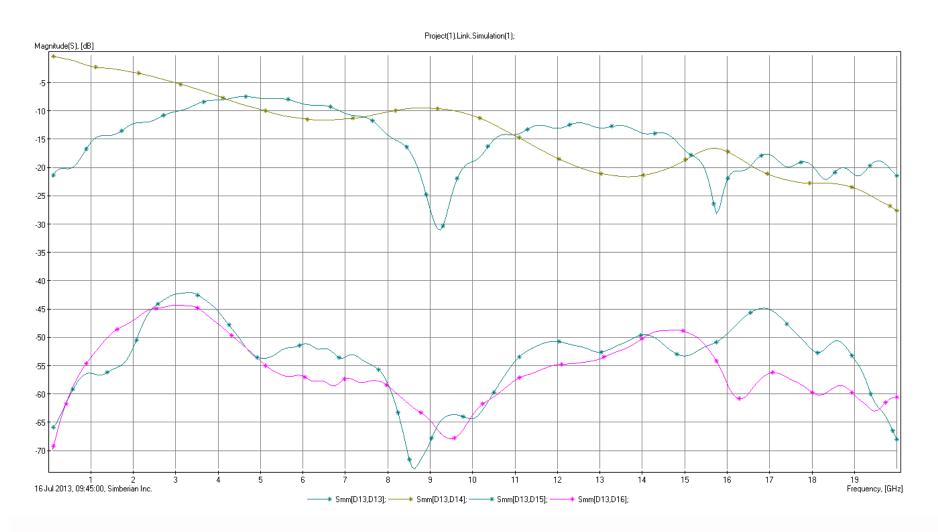




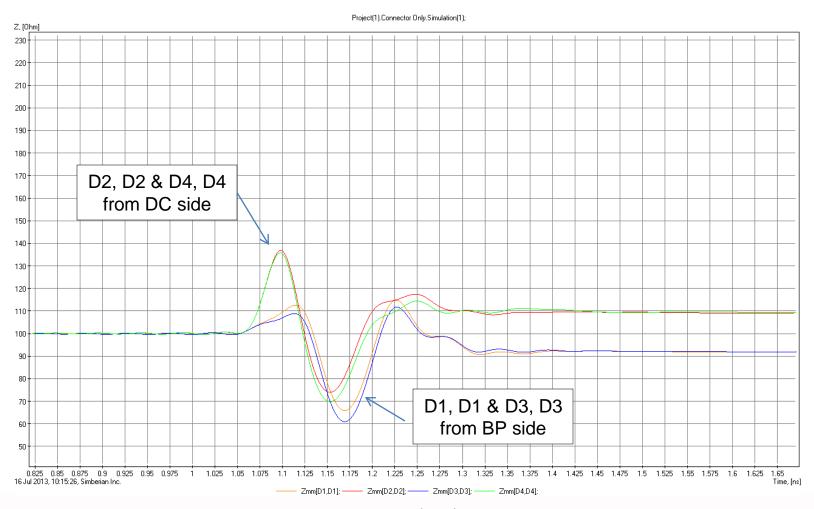




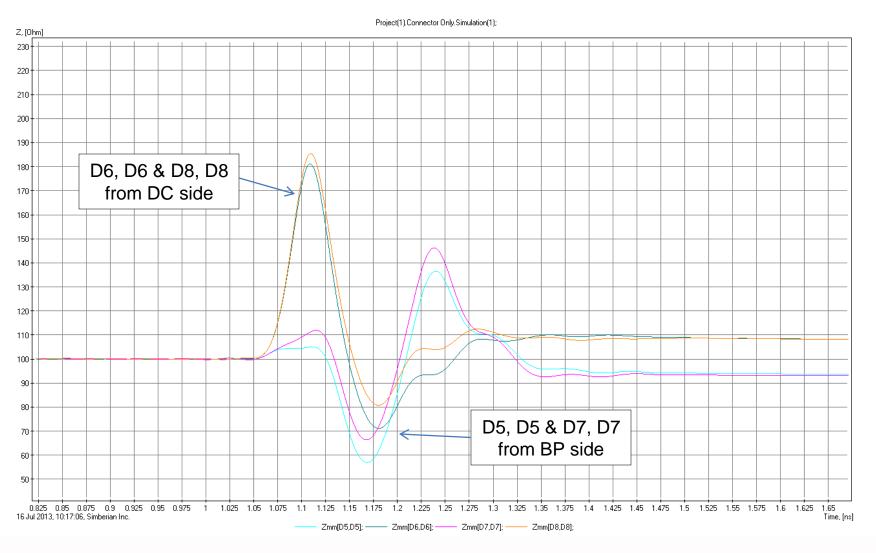




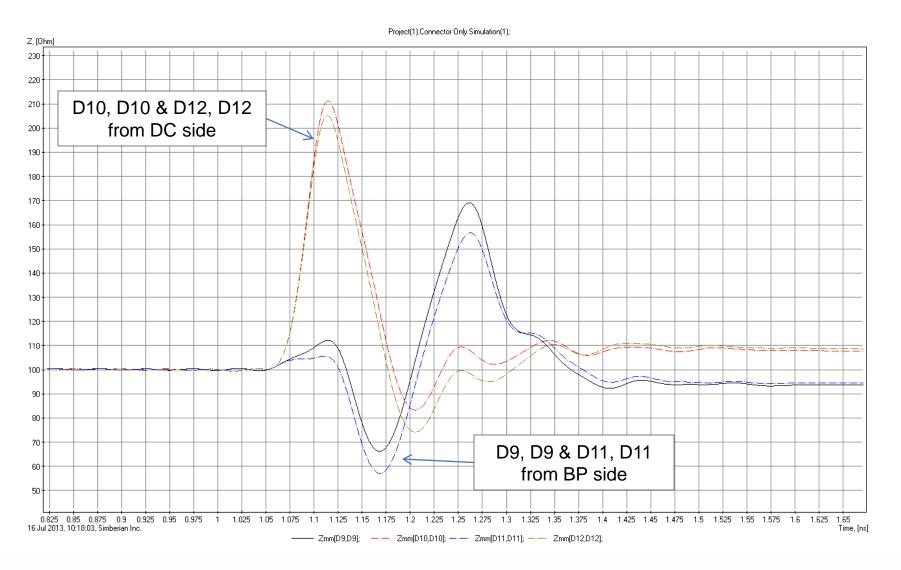




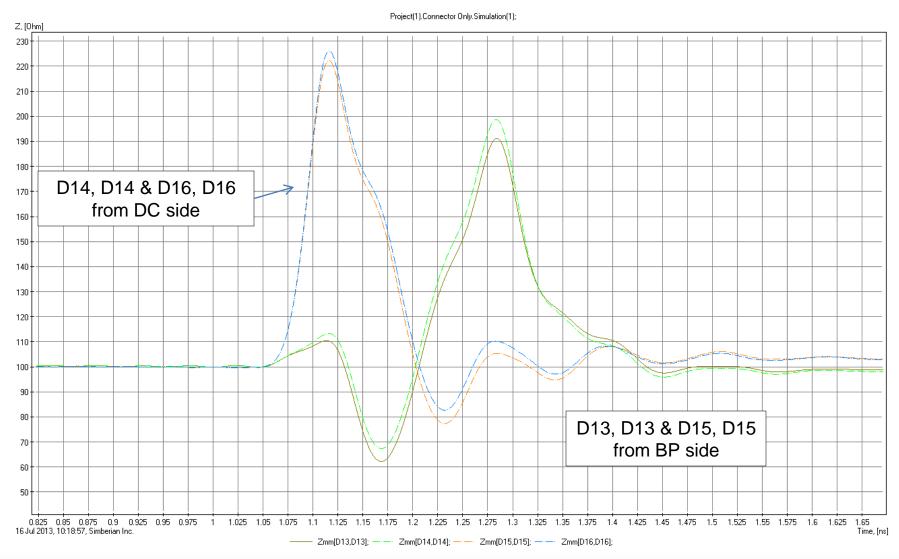




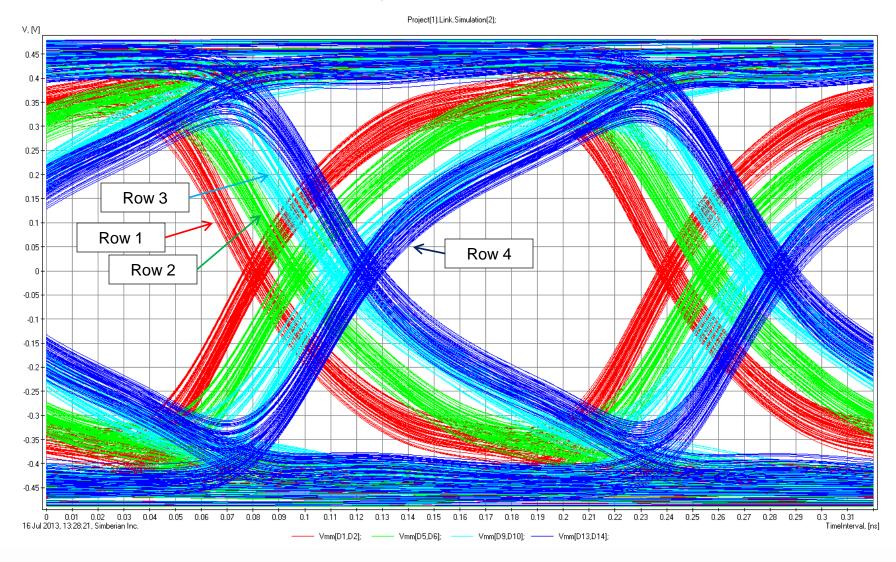




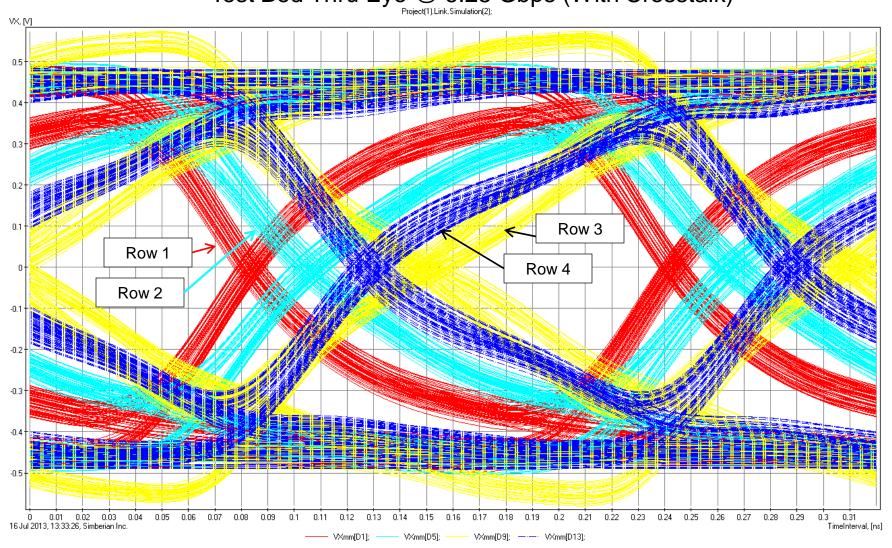


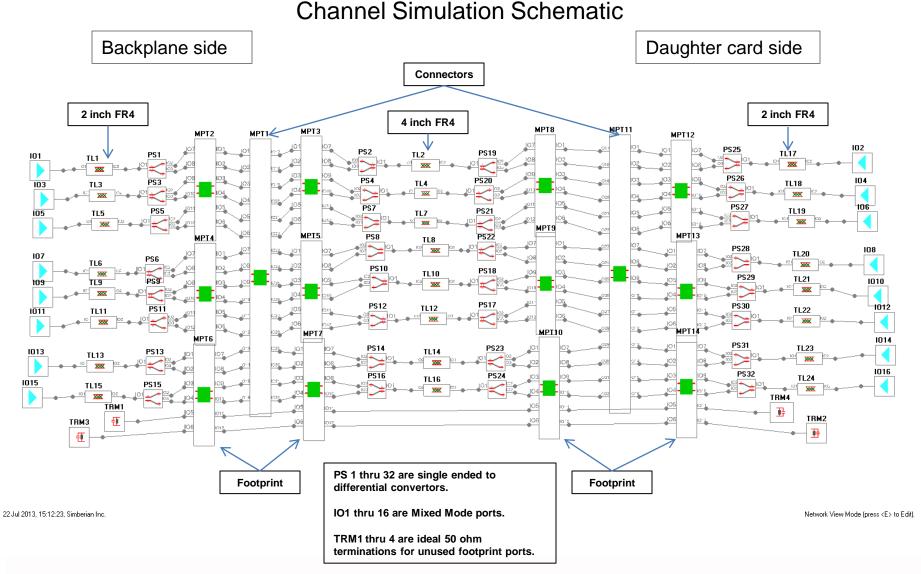


Test Bed Thru Eye @ 6.25 Gbps (No Crosstalk)

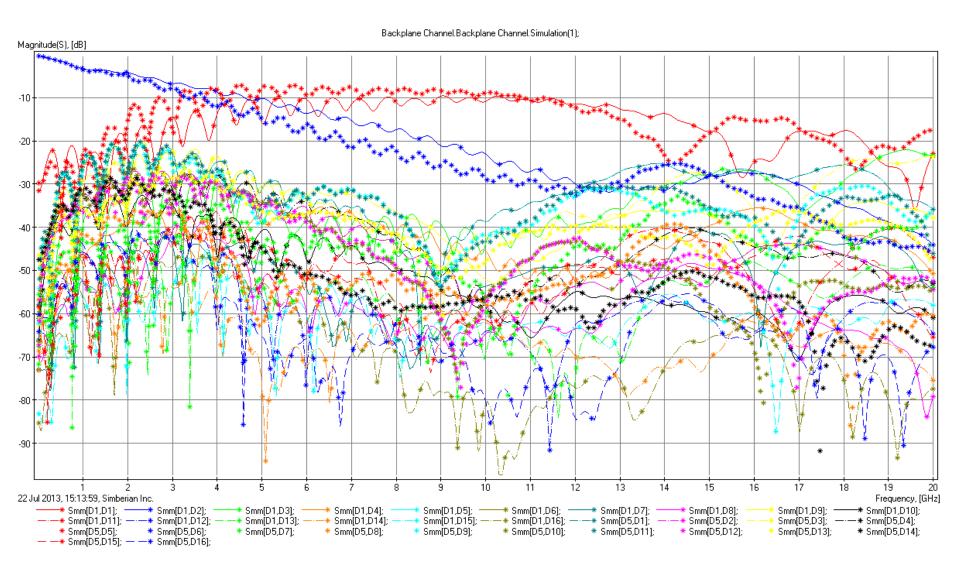


Test Bed Thru Eye @ 6.25 Gbps (With Crosstalk)

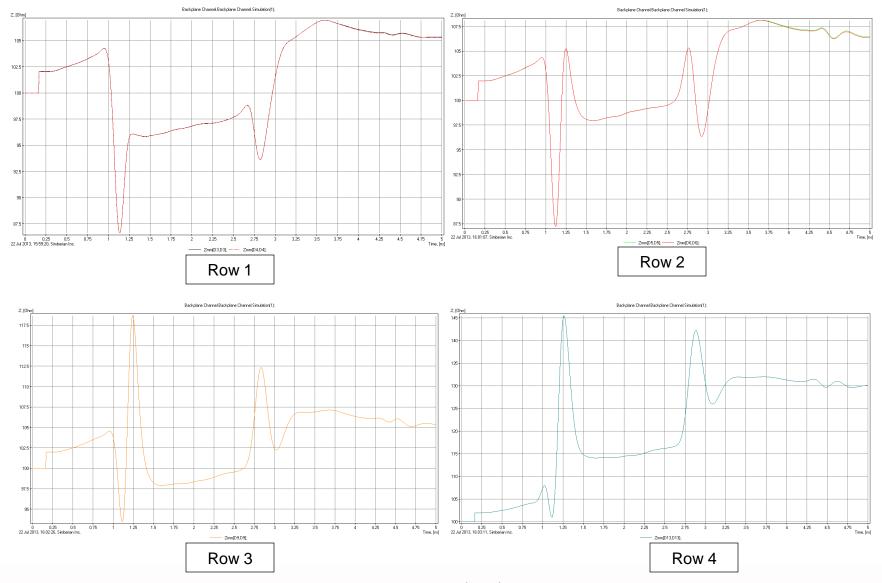




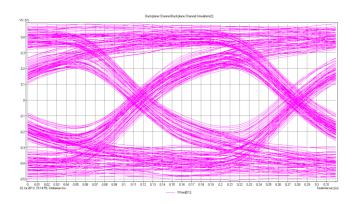
Channel S Parameters



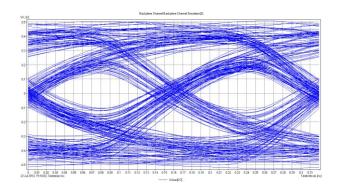
Channel TDR



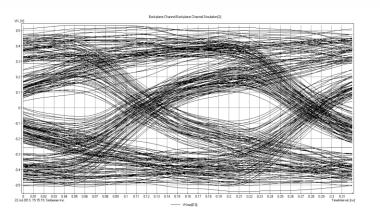
Channel 6.25 Gbps Eye



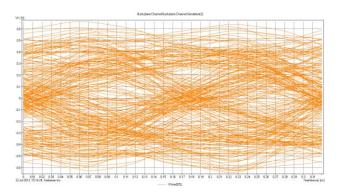
Row 1 – 1 Aggressor



Row 2 – 2 Aggressors

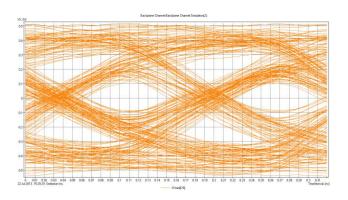


Row 1 – 2 Aggressors

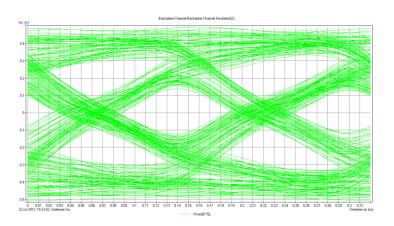


Row 2 – 4 Aggressors

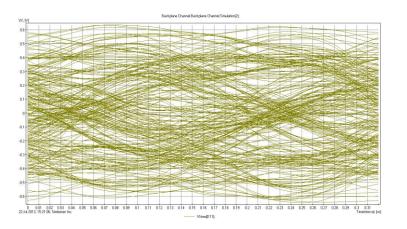
Channel 6.25 Gbps Eye



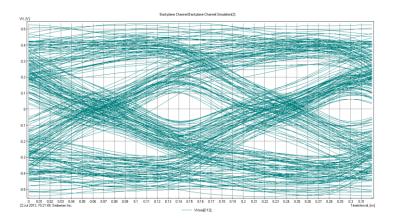
Row 3 – 2 Aggressors



Row 4 – 1 Aggressor



Row 3 – 4 Aggressors



Row 4 – 2 Aggressors