Amphenol
Aerospace

AMPHENOL R-VPX EVOLUTION AND EVOLUTION 2 ROUTING GUIDELINES

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1. Scope

1.1 Intent
The intent of this document is to outline the standard signal trace widths, minimum spacing requirements, and finish hole size requirements for R-VPX Evolution and Evolution 2 product family of interconnect systems when used in differential signal applications and low speed applications.

1.2 Efficient routing
Efficient routing of signal traces between connector patterns improves yields and manufacturability. Spacing between trace/pad and trace/trace needs to be considered to allow for proper feature modifications needed for the inner layer fabrication process. Failure to allow for this may result in lower yields and higher PWB costs.

1.3 Finished Hole Sizes
All finished hole size requirements provided within this document are based on testing completed in FR-4 laminate.

2. Definitions

2.1 Fillets
An extension of the pad at the interface of the trace to the pad that will allow more pad area, in the event that the pad to hole registration compromises the interconnect area. See Figure 1 for details. For further information regarding these routing guidelines, please contact AAO Applications Engineering.

2.2 Foils/Copper Weights
Copper foil is measured in ounces (or weight). Common copper weights are 0.5 ounces, 1 ounce, 1.5 ounces and 2 ounces (3 ounces up to 10 ounces are available for special order). 1 ounce = 0.0014”, 1.5 ounces = 0.0021”, 2 ounces = 0.0028”.

2.3 Pads/Lands/Annular Ring
A pad is the support around a hole. If you see a specification calling out an annular ring of 0.005”, that will mean the amount of the pad left around the hole after processing.

2.4 Spacing
Spacing is the space between two electrical connections; it can be between two lines, two pads, a line and a pad etc.

2.5 Trace/Circuit/Line Width/Lines/Conductor
These are different terms for a connection. If you see the term 0.008” lines, it means the electrical connection from one point to another will measure 0.008” width.

2.6 Backplane
When used within this document refers to the PCB associated with the male connector half of the connector system mounted to a fixed PCB in a chassis.

2.7 Daughtercard
When used within this document refers to the PCB associated with the female connector half of the connector system mounted to a plug-in card in a chassis.

3. Routing Guidelines

3.1 Minimum Spacing
Minimum spacing, specific pad/trace, and trace/trace between all features should be 0.005” (0.127 mm) to allow for manufacturing tolerances.

3.2 Impedance
Consider characteristic impedance (if applicable) when designing to ensure line widths will meet requirements. Please contact AAO Applications Engineering for impedance calculations.

3.3 Copper Weights
Consider copper weights when routing. Higher weights will impact minimum trace widths.

3.4 Fillets
Fillets at the interface (egress) of the trace to the pad are required to improve annular ring when the electrical design requires tight hole to pad configurations.

3.5 Trace Centering
Center all traces between holes to optimize spacing.

3.6 Non Functional Pads
For high speed applications, remove all non-functional pads.

4. Design Rules and Manufacturability Guidelines

4.1 General Design Rules

4.1.1 R-VPX Evolution and Evolution 2 Drill
BP Tail Hole: ISO 0.65 mm (0.0256”) [Evolution backplane]
Nano Tail Hole: ISO 0.45 mm (0.0177”) [Evolution 2 backplane]
Femto Tail Hole: ISO 0.40 mm (0.0157”) [Evolution and Evolution 2 daughtercard]

4.1.2 Footprint
For specific connector footprint see customer use drawings.

4.1.3 Drilled Hole and Copper Thickness
For copper wall thickness requirements and finish hole size reference, see Table 1.

4.2 Daughtercard/Backplane Manufacturability Guidelines

4.2.1 Line Widths, Pad Sizes and Spacing
Line widths, pad sizes and spacing applicable for 1/2 ounce and 1 ounce copper weights.

4.2.2 Filleting
Filleting of pads recommended (to be added by fabricator) for 0.000" annular ring (tangency), see Figure 1.

4.2.3 Minimum PCB Thickness
BP Tail: Recommended minimum pcb thickness of 0.063" (1.6 mm).
Nano and Femto Tail: Recommended minimum pcb thickness of 0.043"
(1.1 mm).

4.2.4 Non-functional pads
Non-functional pads on signal can be removed at designer's option.

4.2.5 Plane Clearances
Plane clearances are applicable for copper weights up to 2 ounces. Please contact AAO Applications Engineering for applications with more than 2 ounce copper.

4.2.6 Surface Traces
Surface traces are not recommended. If surface traces are used refer to the customer drawings for keep-out zones.

5. Routing Guidelines

5.1 Copper Thickness Requirement and Finished Thickness Reference

Finish Type	Copper thickness, in (mm) per side	Drill size, inches (mm)	Typical Finish Thickness	Finished Hole Size, inches (mm)
Solder Finish [1]	0.0010 (0.0254) min BP tail 0.0025 (0.0635) max BP tail 0.0008 (0.020) min Nano tail 0.00275 (0.069) max Nano tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	BP Tail: 0.0256 (0.65) Nano Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	300 to 500 micro inches	BP Tail: 0.0220 +/- 0.002 (0.56 +/- 0.05) Nano Tail: 0.0142 +/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122 +/- 0.002 (0.31+/-0.05)
Immersion Sn (Tin)	0.0010 (0.0254) min BP tail 0.0025 (0.0635) max BP tail 0.0008 (0.020) min Nano tail 0.00275 (0.069) max Nano tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	BP Tail: 0.0256 (0.65) Nano Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	35 to 75 micro inches minimum	BP Tail: 0.0220 +/- 0.002 (0.56 +/- 0.05) Nano Tail: 0.0142 +/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122 +/- 0.002 (0.31 +/- 0.05)
Immersion Ag (Silver)	0.0010 (0.0254) min BP tail 0.0025 (0.0635) max BP tail 0.0008 (0.020) min Nano tail 0.00275 (0.069) max Nano tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	BP Tail: 0.0256 (0.65) Nano Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	4 micro inches minimum	BP Tail: 0.0220 +/- 0.002 (0.56 +/- 0.05) Nano Tail: 0.0142 +/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122 + 0.002/- 0.001 (0.31 + 0.05/- 0.025)

Copper - OSP	0.0010 (0.0254) min BP tail 0.0025 (0.0635) max BP tail 0.0008 (0.020) min Nano tail 0.00275 (0.069) max Nano tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	BP Tail: 0.0256 (0.65) Nano Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	N/A	BP Tail: 0.0220 +/- 0.002 (0.56 +/- 0.05) Nano Tail: 0.0142 +/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122 +/- 0.002 (0.31 +/- 0.05)
Ni Au (Nickel-Gold)	0.0010 (0.0254) min BP tail 0.0025 (0.0635) max BP tail 0.0008 (0.020) min Nano tail 0.00275 (0.069) max Nano tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	BP Tail: 0.0256 (0.65) Nano Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	53 to 210 micro inches Ni-Au compositions combined	BP Tail: 0.0220 +/- 0.002 (0.56 +/- 0.05) Nano Tail: 0.0142 +/- 0.002 (0.36 +/- 0.05) Femto Tail: 0.0122 +/- 0.002 (0.31 +/- 0.05)

Table 1: Copper Thickness Requirement and Finished Thickness Reference

NOTES (Table 1):

1. Solder finish includes: Tin/lead reflowed (plated and reflowed) and HASL. Cu and HASL finished must combine to achieve the finished hole size specified.

Copper thickness per side is an Amphenol requirement. The copper plating must be within specified range in Table 1: Copper Thickness Requirement and Finished Thickness Reference according to the specific Finish Type selected by the end user. Copper plating at the knee of the hole is limited to a maximum of 10% above the average copper wall thickness measured in the working zone, see Figure 1 below, of the plated thru hole, and cannot exceed the MAX copper plating thickness specified in Table 1: Copper Thickness Requirement and Finished Thickness Reference

2. Drill size is an Amphenol requirement. Amphenol requires this drill to be used as outlined in Table 1. The drill size specified does not include a tolerance nor does it include a drilled hole tolerance. These tolerance allowances are included in the overall tolerance outlined in the Finish Hole Size tolerance reference range.
3. Typical Finish Thickness is an Amphenol reference value. Amphenol highlights the reference values on these finishes as a guideline for processing and inspection of PCB holes. Actual finish thicknesses will vary depending on the finish type selected by the end used design guidelines. However, for ENIG, the nickel plating thickness is not a reference but is a requirement.
4. Finish Hole Size is an Amphenol Nominal Value. The Finish Hole Size tolerance for each finish type accounts for the accumulation of tolerances in the actual Drill Hole Diameter as a result of using the specified drill noted in the table above and Finish Thickness over the range of holes in a connector-hole pattern on a PCB. Cu thickness, finish plating thickness, and Drill Size must be adhered to per Amphenol's requirements in this document, but not cumulatively exceeded where these tolerance buildups exceed the finish hole requirements called out.

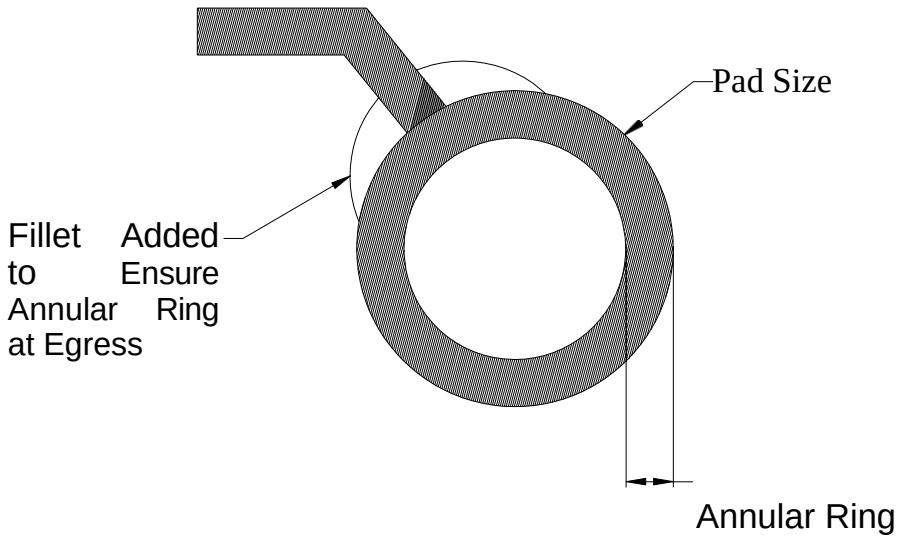

Figure 1: Preferred Fillet

Fillet Diameter equals one half size of plated through hole pad diameter located on a line central to trace so that fillet size equals minimum annular ring plus 0.005” (0.13 mm).

5.2 Drill and Finished Hole Size

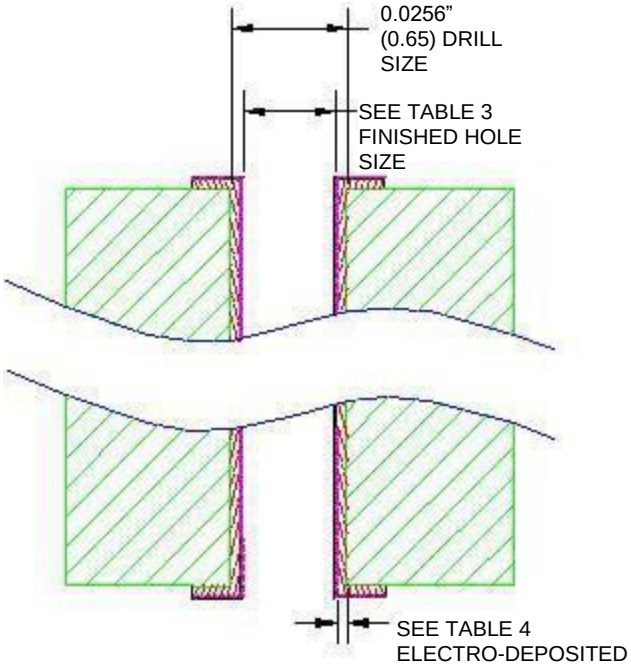

Figure 2: BP Tail (0.0256”) Drill and Finished Hole Size

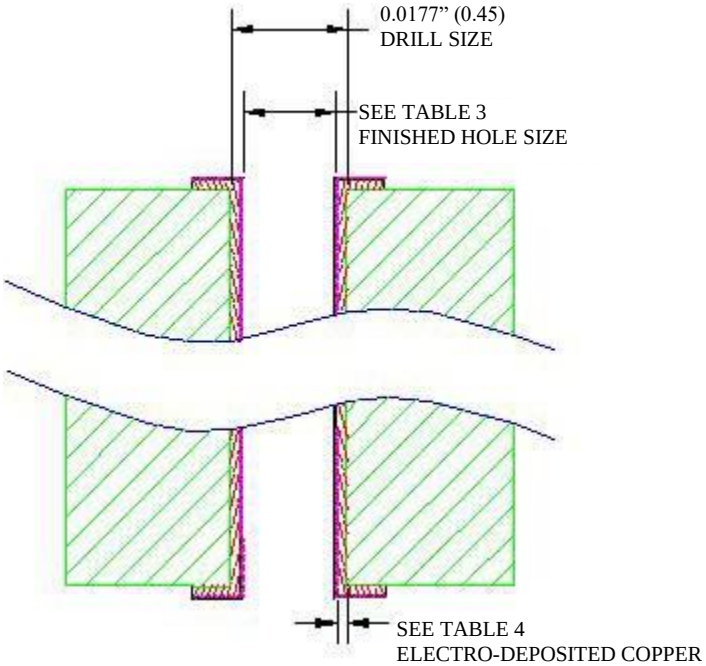

Figure 3: Nano Tail (0.0177”) Drill and Finished Hole Size

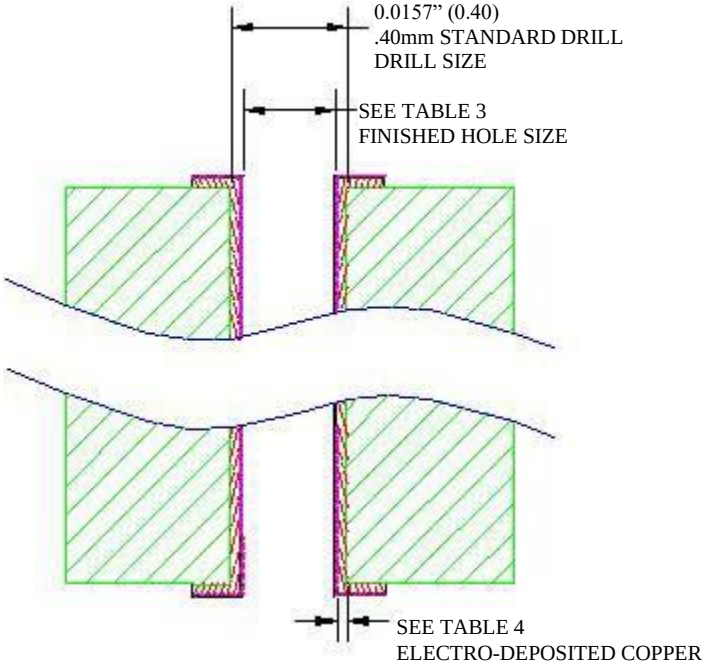

Figure 4: Femto Tail Drill (0.0157”) and Finished Hole Size

5.3 Compliant Pin Critical Zone

The “Critical Working Zone” shown in the following figures is defined as the compliant working zone where the plated through hole requirements must meet the specifications defined within this document. In the “Non Critical Zone”, the plated through hole is allowed to go below the minimum required finish hole size for non-midplane applications. Back drilling is allowed in the “non-critical zone” only.

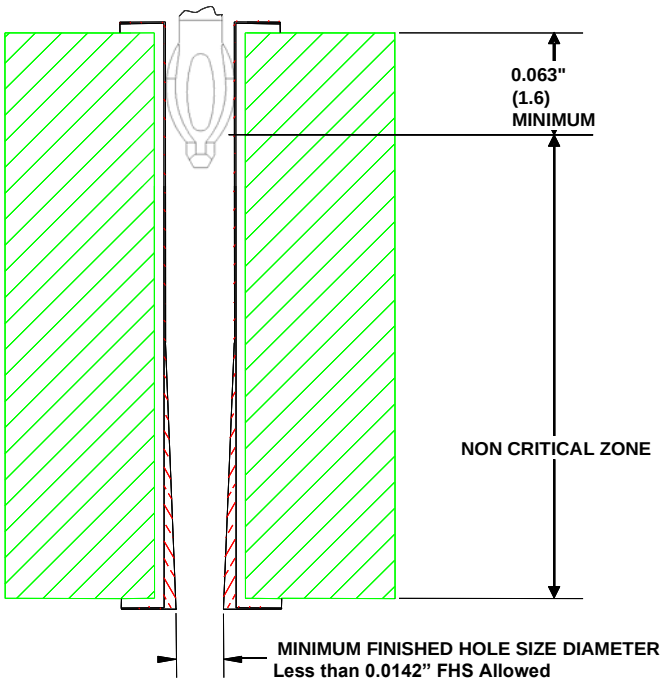

Figure 5: BP Tail (0.0256”) Compliant Pin Critical Zone

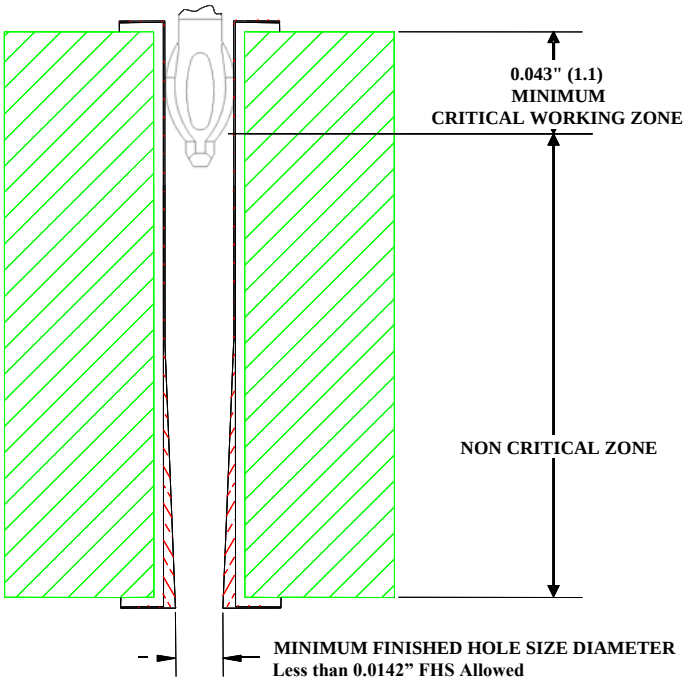

Figure 6: Nano Tail (0.0177") Compliant Pin Critical Zon

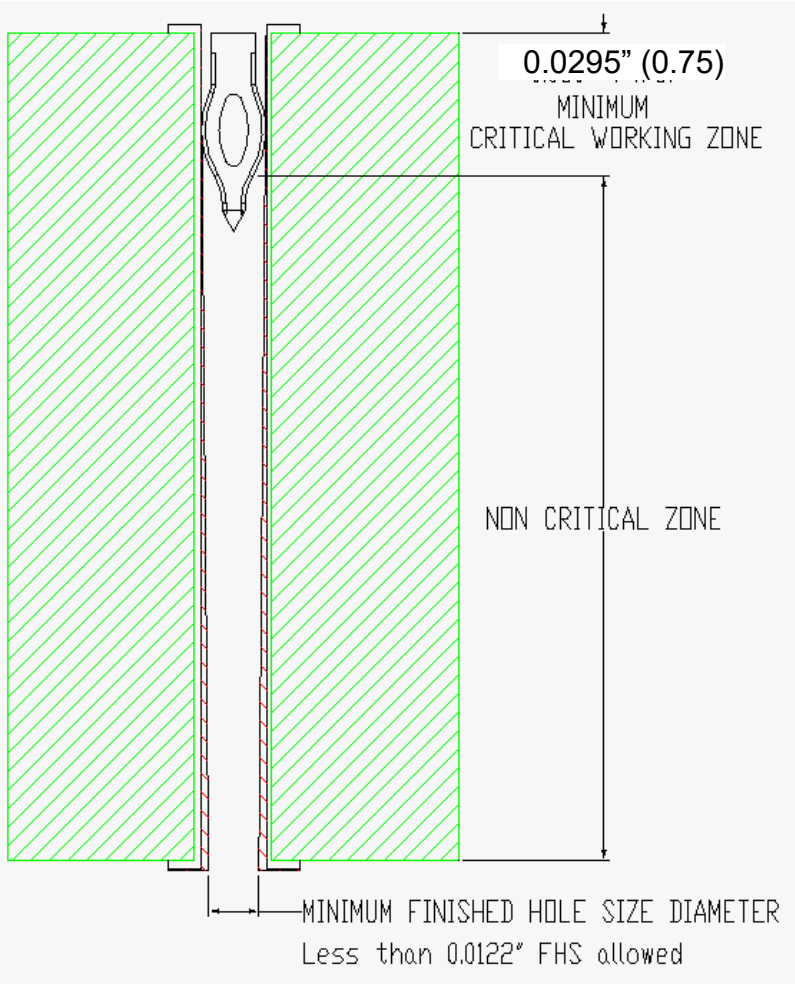

Figure 7: Femto Tail (0.0157") Compliant Pin Critical Zone

5.4 Typical Antipad Geometry

The following describes the nominal antipad design for R-VPX Evolution and Evolution 2. Variations to this design based on stackup design and performance requirements are allowed.

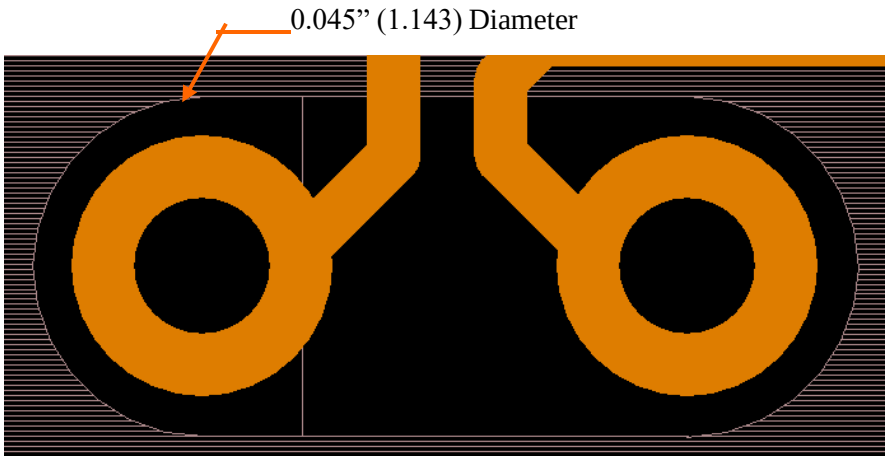

Figure 8: Antipad Clearance – Backplane Connector

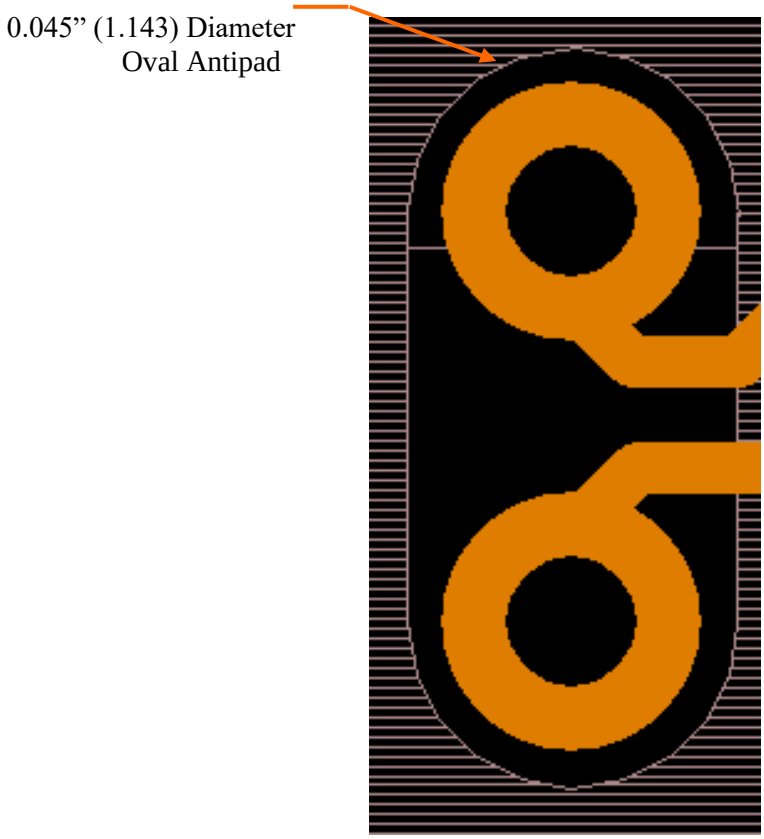

Figure 9: Antipad Clearance – Daughtercard Connector

See also section 5.6.3 and consult AAO regarding usage of elongated antipads for enhanced impedance

5.5 R-VPX Evolution and Evolution 2 Typical High Speed Differential Routing

For complete hole pattern dimensions please refer to the customer use drawings.

5.5.1 Example 1 R-VPX Evolution and Evolution 2 Daughtercard Routing

The available space for routing is determined by the distance between antipads. *There is no secondary routing channel available on the Daughtercard for differential pairs.*

Center to Center	0.0709 (1.8)
- AntiPad Diameter	0.045 (1.143)
= Resulting Space for Traces	0.0259 (0.658)
Line Width	0.006 (0.152)
Space Between Lines	0.006 (0.152)
Resulting Ground Plane Web Overhang on Each Side	0.00395 (0.100)

Table 2: Daughtercard Routing Channel

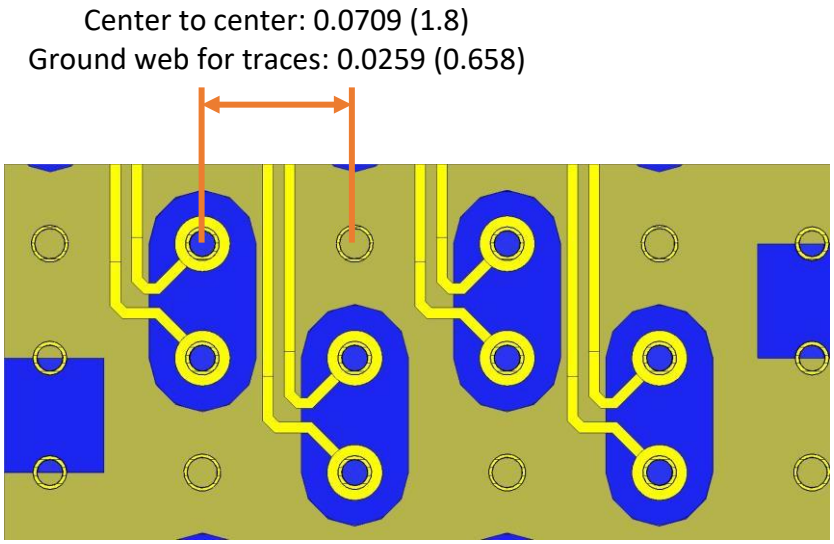

Figure 10: Example Daughtercard High Speed Differential Routing

5.5.2 Example 2 R-VPX Evolution and Evolution 2 Daughtercard Routing

The available space for routing is determined by the distance between antipads. *There is no secondary routing channel available on the Daughtercard for differential pairs.*

Center to Center	0.0709 (1.8)
- AntiPad Diameter	0.045 (1.143)
= Resulting Space for Traces	0.0259 (0.658)
Line Width	0.006 (0.152)
Space Between Lines	0.006 (0.152)
Resulting Ground Plane Web Overhang on Each Side	0.00395 (0.100)

Table 3: Example Daughtercard Routing Channel

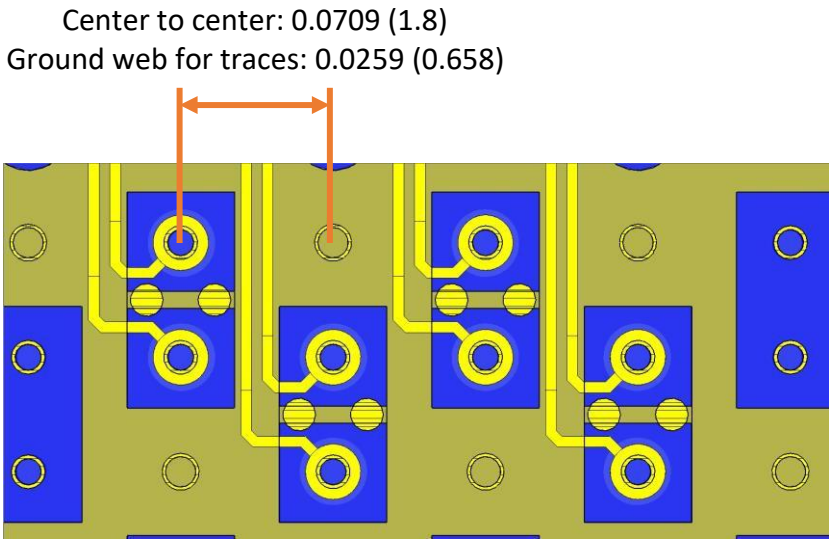

Figure 11: Example Daughtercard High Speed Differential Routing

5.5.3 R-VPX Evolution and Evolution 2 Daughtercard routing – Advanced features for improved signal integrity performance

This footprint assumes the use of individual rectangular antipads as shown in Figure 12. The individual antipads, along with the pair of "shadow vias" greatly improve the footprints common mode performance.

Additionally, the use of the antipad shape shown in Figure 13, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance greatly helps with overall impedance matching and common mode performance.

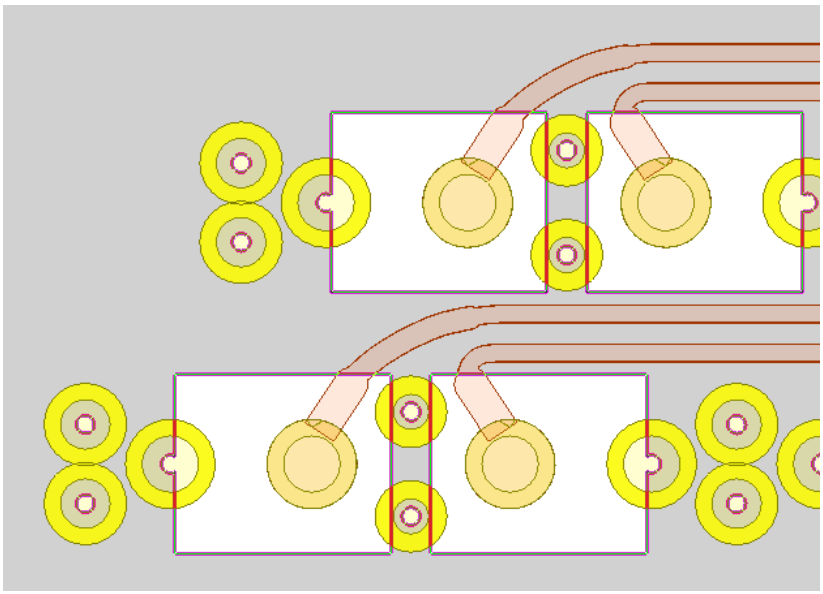

Figure 12: Example Daughtercard Typical High Speed Differential Antipad Design

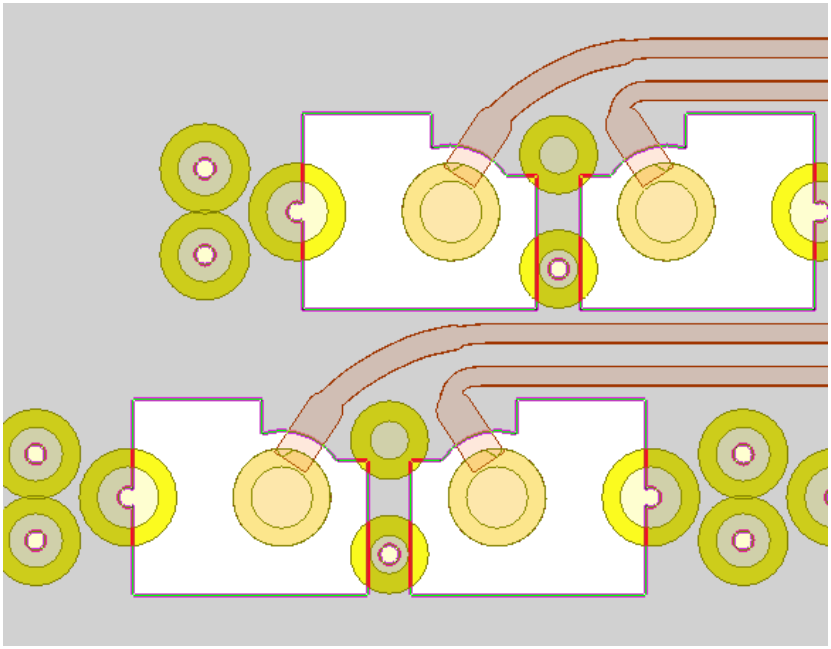

Figure 13: Example Daughtercard Typical High Speed Differential Antipad Design

5.5.4 Example R-VPX Evolution and Evolution 2 Backplane Routing

The amount of space available for routing is determined by the ground plane web in between the antipad clearances.

Center to Center	0.0709 (1.8)
- AntiPad Diameter	0.045 (1.143)
= Resulting Space for Traces	0.0259 (0.658)
Line Width	0.006 (0.152)
Space Between Lines	0.006 (0.152)
Resulting Ground Plane Web Overhang on Each Side	0.00395 (0.100)

Table 4: Example R-VPX Evolution Backplane Routing Channel

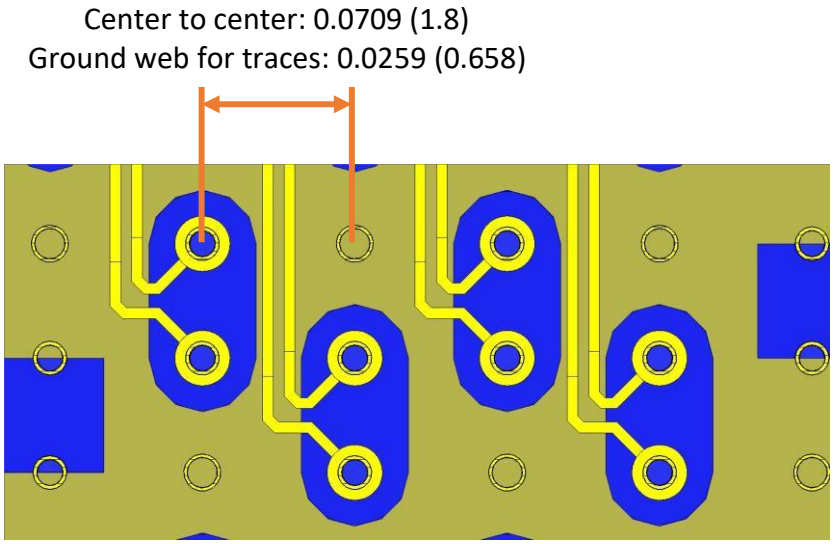

Figure 14: Example Backplane Typical High Speed Differential Routing Ground Plane

5.6.1 Elongated Antipad for Improved Return Loss

The double ground vias between signal pairs in R-VPX Evolution and Evolution 2 allow for elongated antipads that directly pass through the ground vias. There are two ways to achieve this antipad design. The first option, shown in Figure 15, has the antipad cut through the center of the ground vias. In this case a pad is needed at the ground via in order to ensure proper drill location.

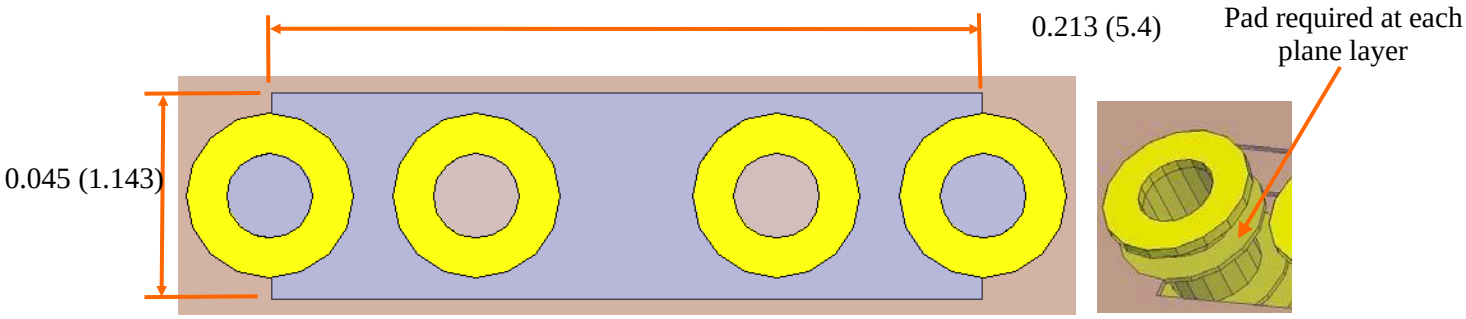

Figure 15: Option 1 Elongated Rectangular Backplane Antipad Clearance

The second option, shown in Figure 16, uses an antipad that is 6mils shorter than the above case. A pad is not needed at the ground via because the drill bit will not wander from the ground via center when it strikes the plane.

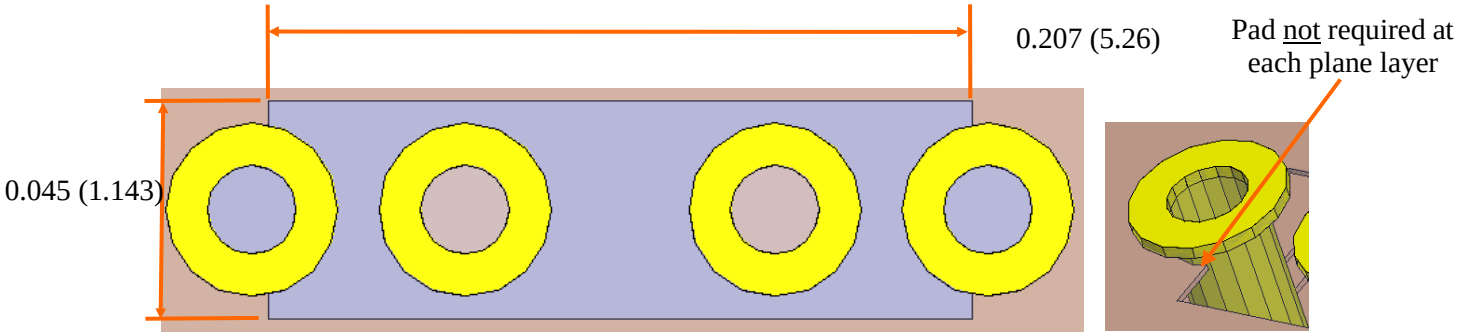

Figure 16: Option 2 Elongated Rectangular Backplane Antipad Clearance

Figure 17 shows the performance improvement in S11 by using the elongated rectangular antipad. This plot is from an HFSS simulation of a 24 layer backplane using Nelco 4000-13 with a 32mil stub.

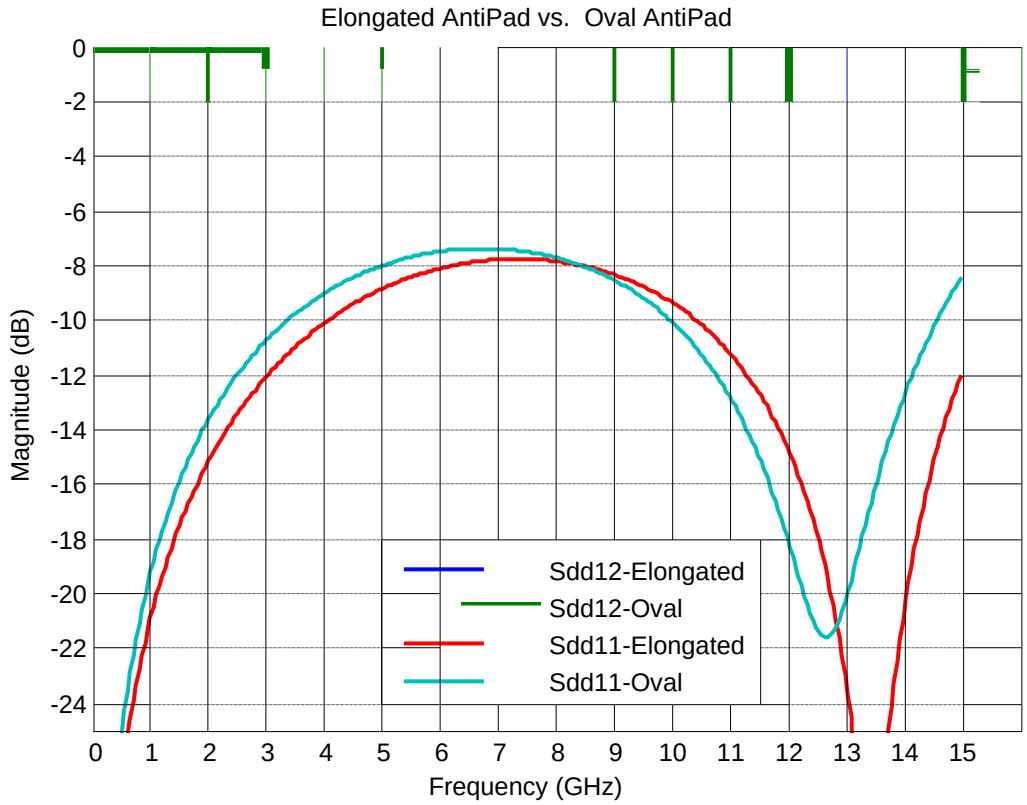

Figure 17: Example Backplane Typical High Speed Differential Routing Ground Plane

5.6.2 Example R-VPX Evolution and Evolution 2 Backplane Routing

The amount of space available for routing is determined by the ground plane web in between the antipad clearances.

Center to Center	0.0709 (1.8)
- AntiPad Diameter	0.045 (1.143)
= Resulting Space for Traces	0.0259 (0.658)
Line Width	0.006 (0.152)
Space Between Lines	0.006 (0.152)
Resulting Ground Plane Web Overhang on Each Side	0.00395 (0.100)

Table 5: Example R-VPX Evolution Backplane Routing Channel

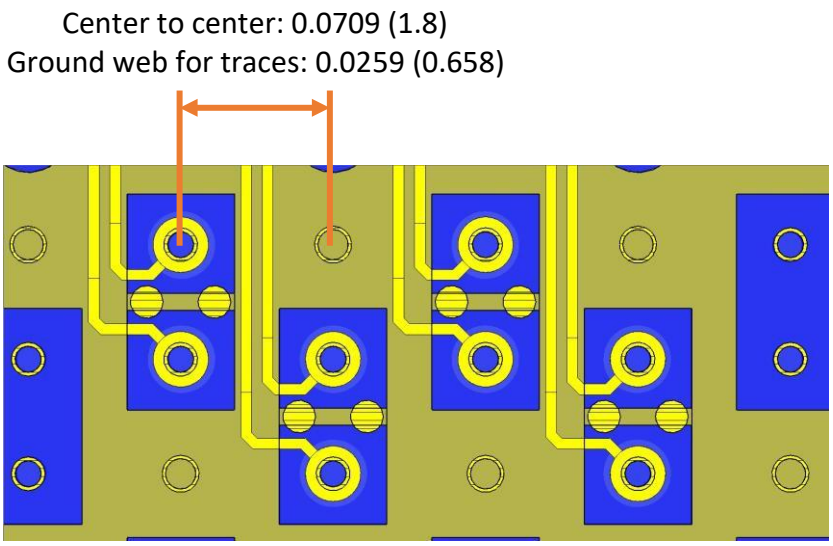

Figure 18: Example Backplane Typical High Speed Differential Routing Ground Plane

5.6.3

This footprint assumes the use of individual rectangular antipads as shown in Figure 19. The individual antipads, along with the pair of "shadow vias" greatly improve the footprints common mode performance.

Additionally, the use of the antipad shape shown in Figure 20, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance greatly helps with overall impedance matching and common mode performance.

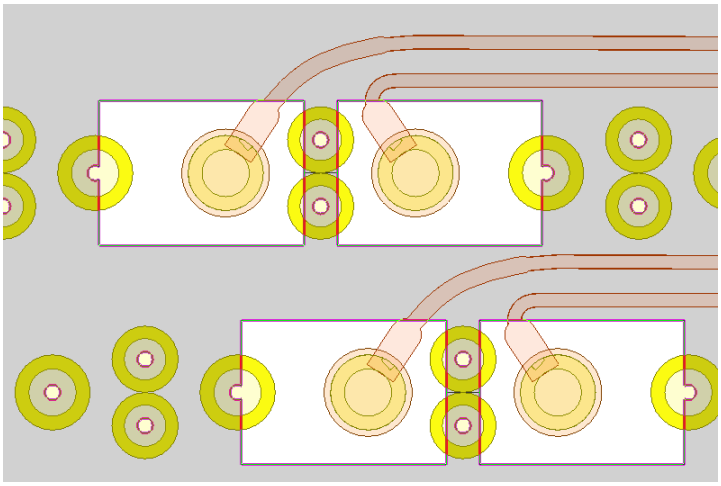

Figure 19: Example Backplane Typical High Speed Differential Antipad Design

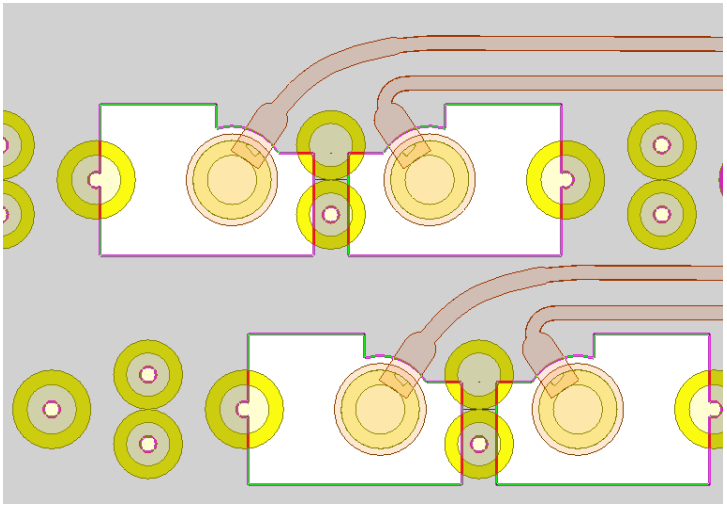

Figure 20: Example Backplane Typical High Speed Differential Antipad Design

5.6.4 Printed Circuit Board Skew Compensation

If the length of one net of a differential pair needs to be increased in order to achieve low skew within the pair, the following picture shows an example of how to achieve this goal.

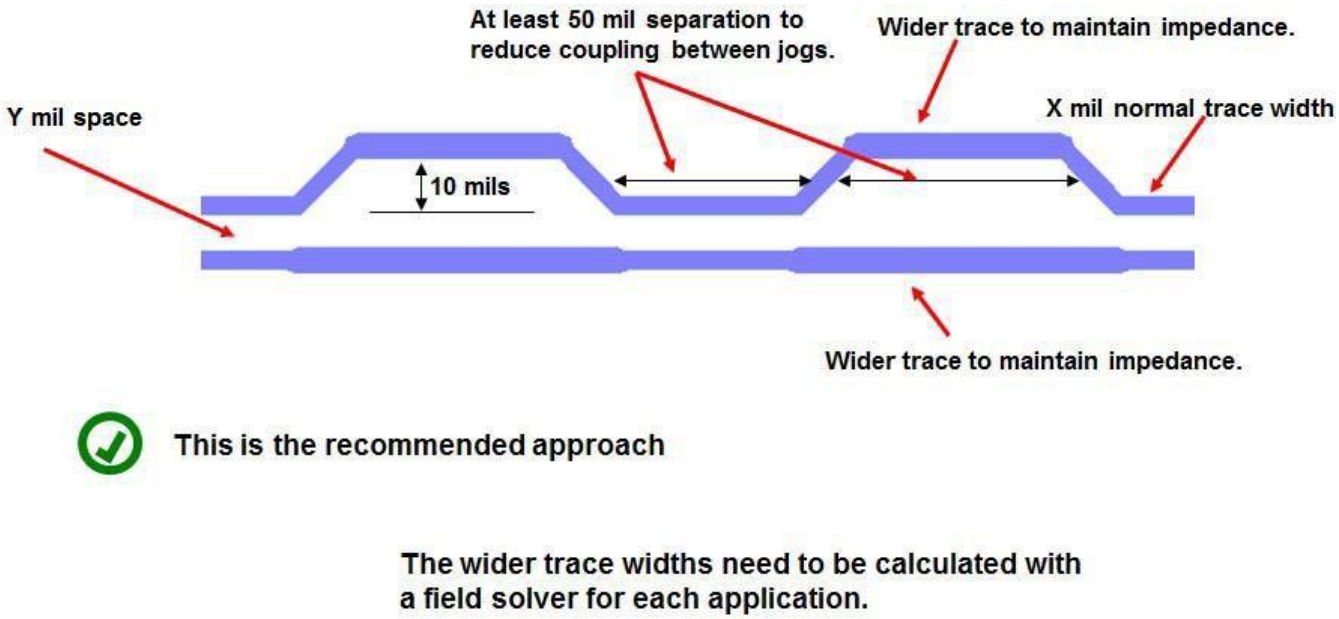

Figure 21: Skew compensation recommended approach

5.6.5 Example R-VPX Evolution and Evolution 2 Daughtercard PCB Ground Via Scheme (Improved Crosstalk)

The grounding scheme shown in Figure 22 makes use of shadow vias surrounding the connector ground via. This in turn improves the crosstalk performance between pairs (pair D9/E9 surrounded by pairs on columns 7 through 10) as shown in Figure 23. This simulated data was taken from a 16 layer 93 mil thick daughtercard PCB using Megtron 6.

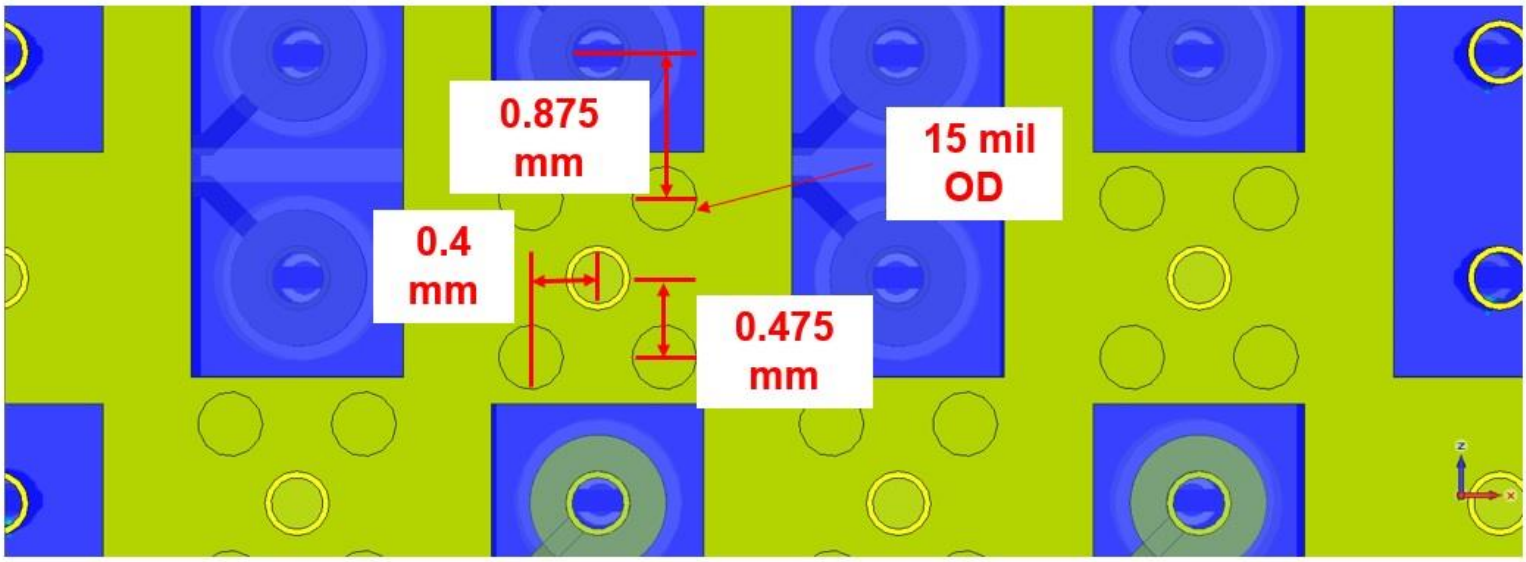

Figure 22: Daughtercard PCB ground via dimensions

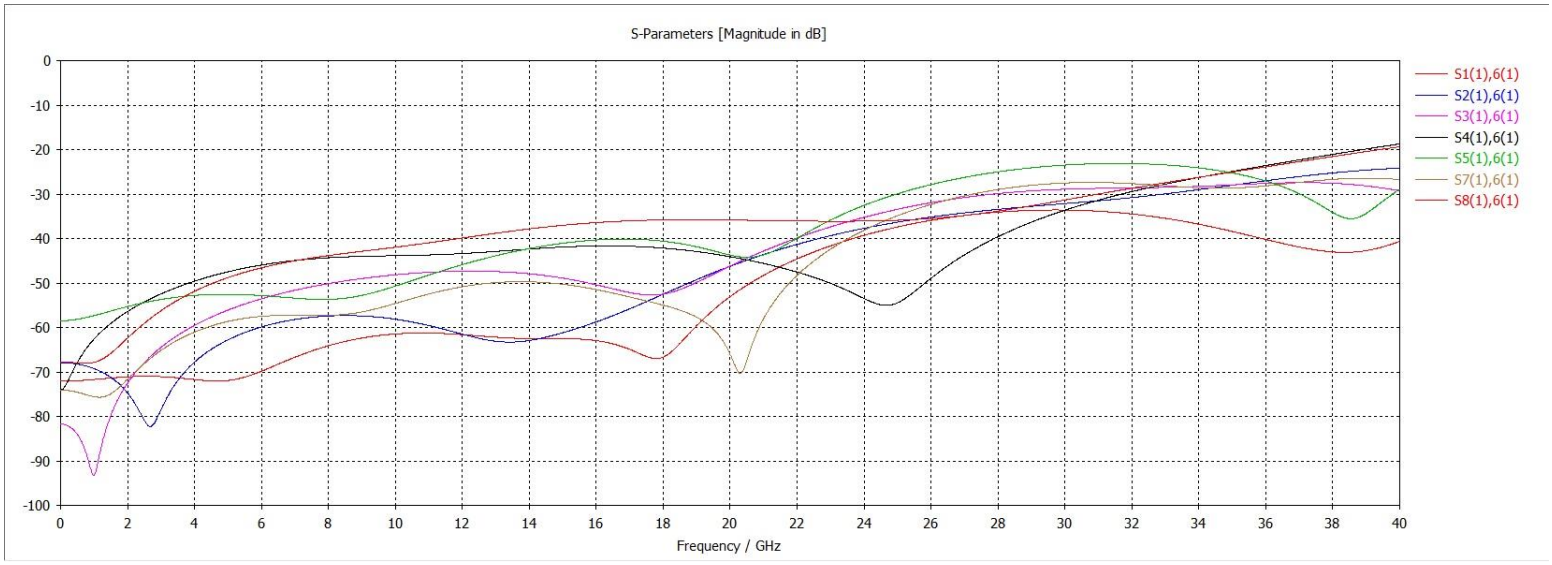

Figure 23: Daughtercard PCB near-end crosstalk

5.6.6 Example R-VPX Evolution 2 Backplane PCB Ground Via Scheme (Improved Crosstalk)

The grounding scheme shown in Figure 24 makes use of shadow vias surrounding the connector ground vias. This in turn improves the crosstalk performance between pairs (pair E9/F9 surrounded by pairs on columns 7 through 10) as shown in Figure 25. This simulated data was taken from a 16 layer 250 mil thick backplane PCB using Megtron 6.

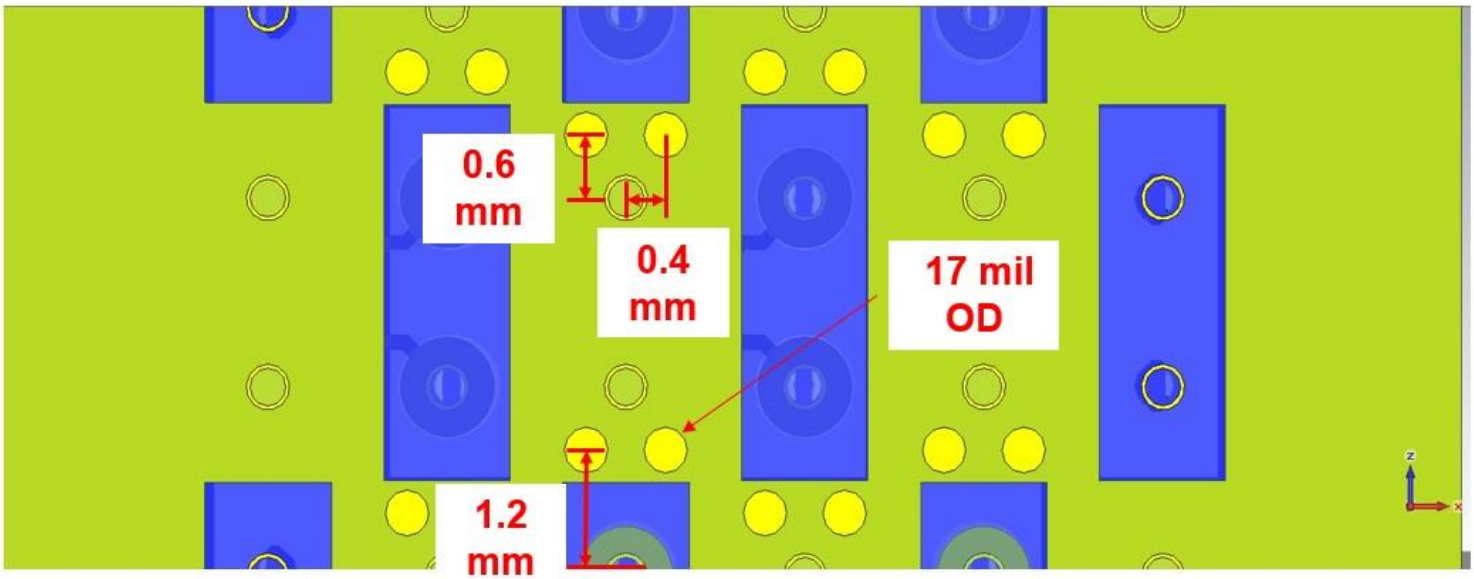

Figure 24: Backplane PCB ground via dimensions

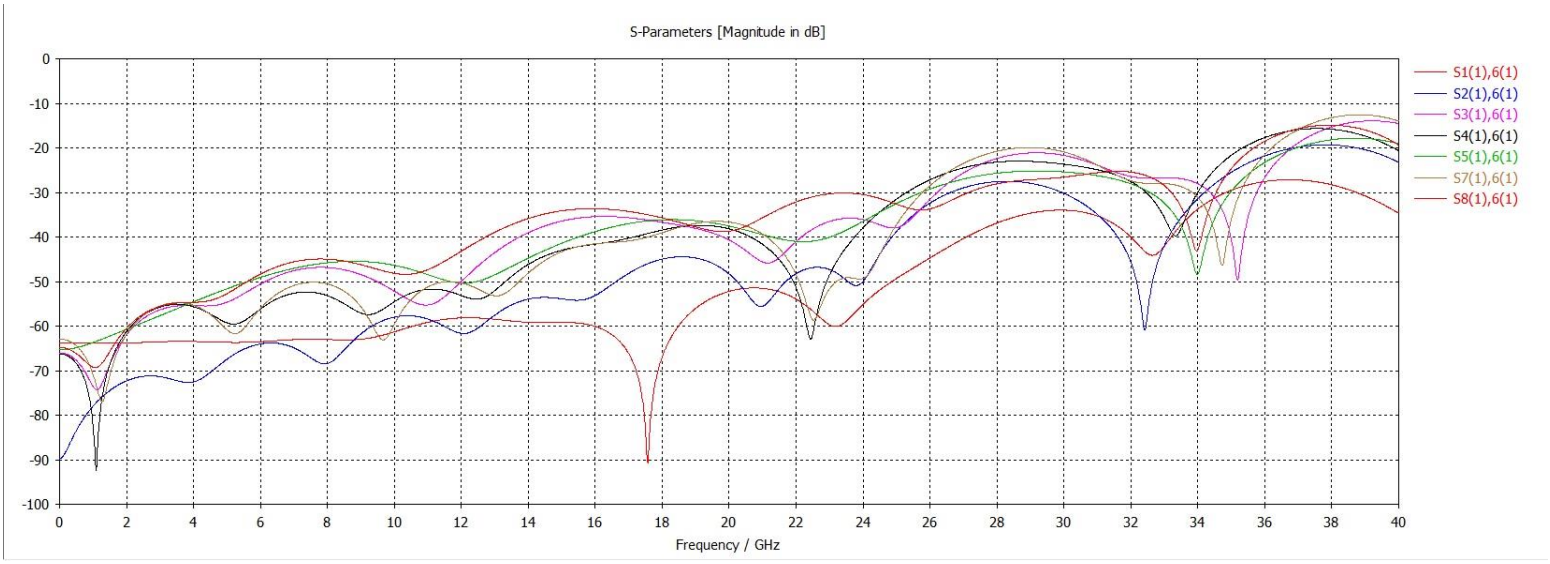

Figure 25: Backplane PCB near-end crosstalk