24 Channel Copper and Fiber Network Switch up to 100G

12 Channel 100GBase-SR4 + 12 Channel 16Base-T, CF-02WA00-42X

DESCRIPTION

The 24 Channel Copper and Fiber Network Switch up to 100G is a reliable, high-performance switching solution designed for stable and efficient network connectivity in enterprise, industrial, or commercial environments. Designed to support 12 channels of 100GBase-SR4 plus 12 channels 16Base-T and engineered for continuous operation, it delivers fast data transmission, low latency, and dependable traffic management to support modern networking demands.

Built with a robust hardware design, this switch ensures consistent performance under heavy workloads while maintaining secure and orderly data flow across connected devices. Its compact form factor allows flexible deployment in network cabinets or control systems, making it suitable for both new installations and network upgrades.

Ideal for applications requiring dependable connectivity, the switch supports scalable network expansion and helps maintain smooth, uninterrupted communication across your infrastructure.

FEATURES

- High-performance network switching for reliable data transmission
- Robust and durable hardware design for continuous operation
- Efficient traffic handling to reduce congestion and latency
- Compact form factor for easy integration into existing network setups
- Supports stable connectivity across multiple network devices
- Designed for scalable network expansion
- Suitable for enterprise, commercial, and industrial networking environments
- Ensure consistent and uninterrupted network performance
- Improves overall network efficiency and data flow reliability
- Reduces downtime through dependable, long-term operation
- Simplified installation and network upgrades
- Adapts easily to growing network requirements

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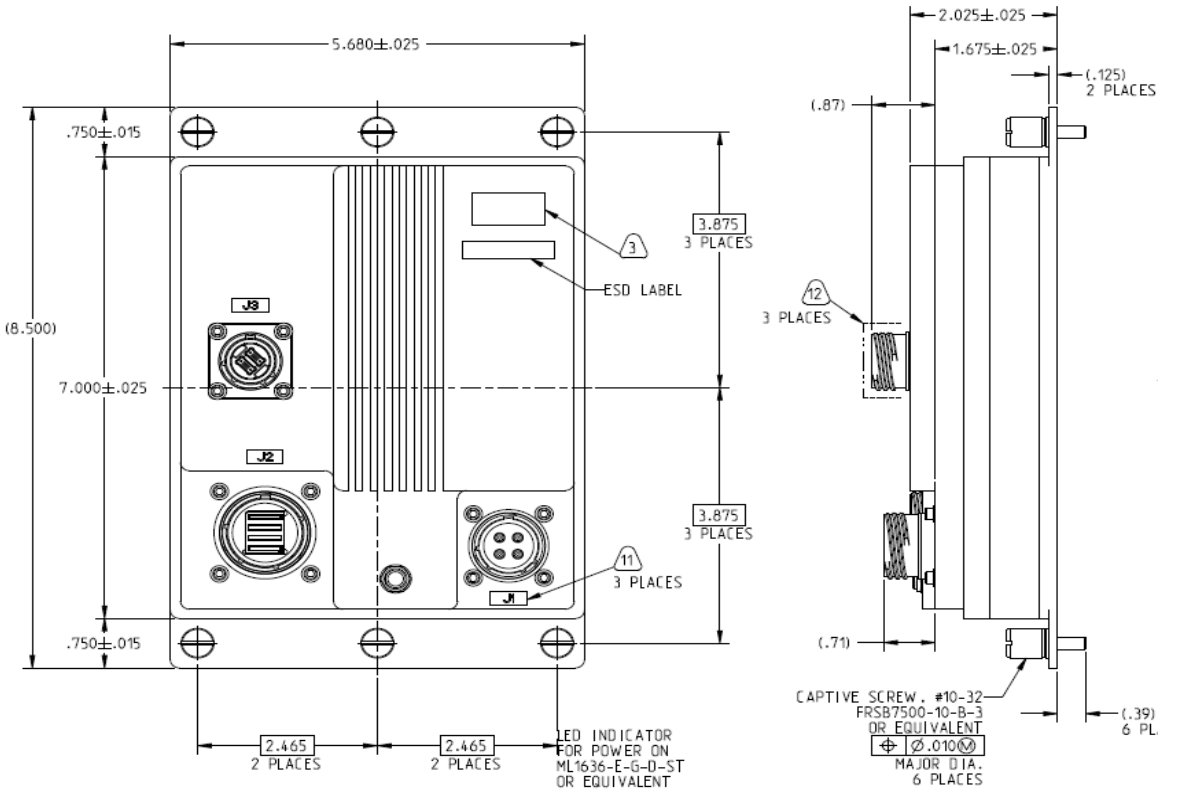
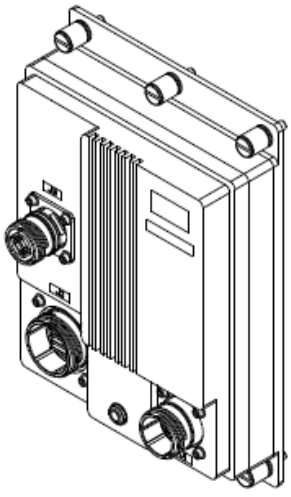
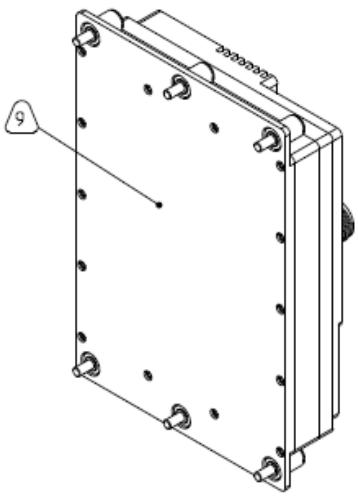
DIMENSIONS & I/O

CF-02WA00-42X

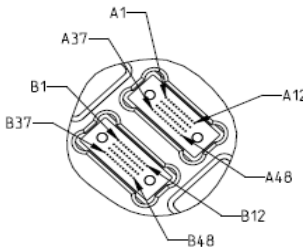




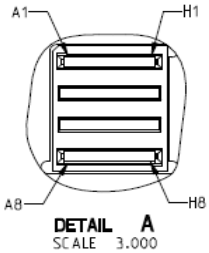
FRONT ISOMETRIC VIEW
SCALE 0.600



REAR ISOMETRIC VIEW
SCALE 0.600



DETAIL B
SCALE 5.000



DETAIL A
SCALE 3.000

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CHARTS

J1 I/O, J2 I/O, J3 I/O

J1 I/O CHART	
PIN ID	DESCRIPTION
A	28VDC_IN
B	28VDC_RTN
C	SAFETY GROUND CHASSIS
D	N/C
SHELL	CHASSIS

J2 I/O CHART								
	A	B	C	D	E	F	G	H
1	DISCRETE1	GND	DP1P	DP1N	GND	DP2P	DP2N	GND
2	GND	DP3P	DP3N	GND	DP4P	DP4N	GND	DISCRETE2
3	DISCRETE3	GND	DP5P	DP5N	GND	DP6P	DP6N	GND
4	GND	DP7P	DP7N	GND	DP8P	DP8N	GND	DISCRETE4
5	DISCRETE5	GND	DP9P	DP9N	GND	DP10P	DP10N	GND
6	GND	DP11P	DP11N	GND	DP12P	DP12N	GND	DISCRETE6
7	DISCRETE7	GND	DP13P	DP13N	GND	DP14P	DP14N	GND
8	GND	DP15P	DP15N	GND	DP16P	DP16N	GND	DISCRETE8

J3 I/O CHART							
PIN ID	DESCRIPTION	PIN ID	DESCRIPTION	PIN ID	DESCRIPTION	PIN ID	DESCRIPTION
A1	CH1_100GBASE-SR4_TX1	A25	CH4_100GBASE-SR4_TX1	B1	CH7_100GBASE-SR4_TX1	B25	CH10_100GBASE-SR4_TX1
A2	CH1_100GBASE-SR4_TX2	A26	CH4_100GBASE-SR4_TX2	B2	CH7_100GBASE-SR4_TX2	B26	CH10_100GBASE-SR4_TX2
A3	CH1_100GBASE-SR4_TX3	A27	CH4_100GBASE-SR4_TX3	B3	CH7_100GBASE-SR4_TX3	B27	CH10_100GBASE-SR4_TX3
A4	CH1_100GBASE-SR4_TX4	A28	CH4_100GBASE-SR4_TX4	B4	CH7_100GBASE-SR4_TX4	B28	CH10_100GBASE-SR4_TX4
A5	CH2_100GBASE-SR4_TX1	A29	CH5_100GBASE-SR4_TX1	B5	CH8_100GBASE-SR4_TX1	B29	CH11_100GBASE-SR4_TX1
A6	CH2_100GBASE-SR4_TX2	A30	CH5_100GBASE-SR4_TX2	B6	CH8_100GBASE-SR4_TX2	B30	CH11_100GBASE-SR4_TX2
A7	CH2_100GBASE-SR4_TX3	A31	CH5_100GBASE-SR4_TX3	B7	CH8_100GBASE-SR4_TX3	B31	CH11_100GBASE-SR4_TX3
A8	CH2_100GBASE-SR4_TX4	A32	CH5_100GBASE-SR4_TX4	B8	CH8_100GBASE-SR4_TX4	B32	CH11_100GBASE-SR4_TX4
A9	CH3_100GBASE-SR4_TX1	A33	CH6_100GBASE-SR4_TX1	B9	CH9_100GBASE-SR4_TX1	B33	CH12_100GBASE-SR4_TX1
A10	CH3_100GBASE-SR4_TX2	A34	CH6_100GBASE-SR4_TX2	B10	CH9_100GBASE-SR4_TX2	B34	CH12_100GBASE-SR4_TX2
A11	CH3_100GBASE-SR4_TX3	A35	CH6_100GBASE-SR4_TX3	B11	CH9_100GBASE-SR4_TX3	B35	CH12_100GBASE-SR4_TX3
A12	CH3_100GBASE-SR4_TX4	A36	CH6_100GBASE-SR4_TX4	B12	CH9_100GBASE-SR4_TX4	B36	CH12_100GBASE-SR4_TX4
A13	CH1_100GBASE-SR4_RX1	A37	CH4_100GBASE-SR4_RX1	B13	CH7_100GBASE-SR4_RX1	B37	CH10_100GBASE-SR4_RX1
A14	CH1_100GBASE-SR4_RX2	A38	CH4_100GBASE-SR4_RX2	B14	CH7_100GBASE-SR4_RX2	B38	CH10_100GBASE-SR4_RX2
A15	CH1_100GBASE-SR4_RX3	A39	CH4_100GBASE-SR4_RX3	B15	CH7_100GBASE-SR4_RX3	B39	CH10_100GBASE-SR4_RX3
A16	CH1_100GBASE-SR4_RX4	A40	CH4_100GBASE-SR4_RX4	B16	CH7_100GBASE-SR4_RX4	B40	CH10_100GBASE-SR4_RX4
A17	CH2_100GBASE-SR4_RX1	A41	CH5_100GBASE-SR4_RX1	B17	CH8_100GBASE-SR4_RX1	B41	CH11_100GBASE-SR4_RX1
A18	CH2_100GBASE-SR4_RX2	A42	CH5_100GBASE-SR4_RX2	B18	CH8_100GBASE-SR4_RX2	B42	CH11_100GBASE-SR4_RX2
A19	CH2_100GBASE-SR4_RX3	A43	CH5_100GBASE-SR4_RX3	B19	CH8_100GBASE-SR4_RX3	B43	CH11_100GBASE-SR4_RX3
A20	CH2_100GBASE-SR4_RX4	A44	CH5_100GBASE-SR4_RX4	B20	CH8_100GBASE-SR4_RX4	B44	CH11_100GBASE-SR4_RX4
A21	CH3_100GBASE-SR4_RX1	A45	CH6_100GBASE-SR4_RX1	B21	CH9_100GBASE-SR4_RX1	B45	CH12_100GBASE-SR4_RX1
A22	CH3_100GBASE-SR4_RX2	A46	CH6_100GBASE-SR4_RX2	B22	CH9_100GBASE-SR4_RX2	B46	CH12_100GBASE-SR4_RX2
A23	CH3_100GBASE-SR4_RX3	A47	CH6_100GBASE-SR4_RX3	B23	CH9_100GBASE-SR4_RX3	B47	CH12_100GBASE-SR4_RX3
A24	CH3_100GBASE-SR4_RX4	A48	CH6_100GBASE-SR4_RX4	B24	CH9_100GBASE-SR4_RX4	B48	CH12_100GBASE-SR4_RX4

SOFTWARE FEATURES

- **Stacking**
- Stacking Ring Topology
- Stacking Chain Topology
- Stacking Members and Unit ID
- Removing and Replacing Stacking Members
- Exchanging Stacking Members
- Switching the Stacking Master
- **Configuring System Time**
- Configuring Daylight Savings Time
- Configuring SNTP
- Polling for Unicast Time Information
- Polling for Anycast Time Information
- Broadcast Time Information
- Defining SNTP Settings
- **Configuring Device Security**
- Configuring Management Security
- Configuring Authentication Methods
- Defining Access Profiles
- Defining Profile Rules
- Defining Authentication Profiles
- Mapping Authentication Methods
- Defining RADIUS Settings
- Defining TACACS+ Authentication
- Configuring Passwords
- Defining Local Users
- Defining Line Passwords
- Defining Enable Passwords
- Configuring Network Security
- Network Security Overview
- Port-Based Authentication
- Advanced Port-Based Authentication
- Defining Port Authentication Properties
- Defining Port Authentication
- Configuring Multiple Hosts
- Defining Authentication Hosts
- Viewing EAP Statistics
- Defining Access Control Lists
- Defining IP Based Access Control Lists
- Defining MAC Based Access Control Lists
- Binding Device Security ACLs
- Managing Port Security
- Enabling Storm Control
- **Configuring System Logs**
- Defining General Log Properties
- Viewing Memory Logs
- Viewing Flash Logs
- Defining System Log Servers
- **Configuring Interfaces**
- Configuring Ports
- Aggregating Ports
- Configuring LACP
- Configuring VLANs
- Defining VLAN Properties
- Defining VLAN Membership
- Defining VLAN Interface Settings
- Configuring GARP
- Defining GARP
- Defining GVRP
- Viewing GVRP Statistics
- **Defining IP Addresses**
- Configuring IP Addressing
- Defining IP Addresses
- Defining ARP
- Defining Domain Name Servers
- Defining DNS Servers
- Defining DNS Host Mapping
- **Defining the Forwarding Database**
- Defining the Forwarding Database
- Defining Access Profiles
- **Configuring Spanning Tree**
- Defining Classic Spanning Tree
- Defining STP on Interfaces
- Defining Rapid Spanning Tree
- Defining Multiple Spanning Tree
- Defining MSTP Instance Settings
- Defining MSTP Interface Settings
- **Configuring SNMP**
- SNMP v1 and v2c
- SNMP v3
- Configuring SNMP Security
- Defining SNMP Security
- Defining SNMP View
- Defining SNMP Group Profiles
- Defining SNMP Group Members
- Defining SNMP Communities
- SNMP Communities Basic Table
- SNMP Communities Advanced Table
- Configuring SNMP Notifications
- Defining SNMP Notification Global Parameters
- Defining SNMP Notification Filters
- Defining SNMP Notification Recipients
- SNMPv1,2c Notification Recipients
- SNMPv3 Notification Recipients
- **Configuring Multicast Forwarding**
- Multicast Forwarding
- Typical Multicast Setup
- Multicast Operation
- Multicast Registration
- Multicast Address Properties
- Defining Multicast Properties
- Adding MAC Group Address
- Adding IP Multicast Groups
- Configuring IGMP Snooping
- Configuring MLD Snooping
- Viewing IGMP/MLD IP Multicast Groups
- Defining Multicast Router Ports
- Defining Forward All Multicast
- Defining Unregistered Multicast Settings
- **Managing System Files**
- Downloading System Files
- Firmware Download
- Configuration Download
- Uploading System Files
- Upload Type
- Software Image Upload
- Configuration Upload
- Copying Files
- Restoring the Default Configuration File
- **Configuring Quality of Service**
- Quality of Service Overview
- VPT Classification Information
- CoS Services
- Defining General QoS Settings
- Configuring QoS General Settings
- Restoring Factory Default QoS Interface Settings
- Defining Queues
- Defining Bandwidth Settings
- Mapping CoS Values to Queues
- Mapping DSCP Values to Queues
- Defining QoS Basic Mode
- Defining Basic Mode Settings
- Rewriting Basic Mode DSCP Values
- Defining QoS Advanced Mode
- Setting Policy Binding
- **Managing Device Diagnostics**
- Configuring Port Mirroring
- **Viewing Statistics**
- Viewing Interface Statistics
- Viewing Interface Statistics
- Receive Statistics
- Transmit Statistics
- Viewing Etherlike Statistics
- Managing RMON Statistics
- Viewing RMON Statistics
- Configuring RMON History
- Defining RMON History Control
- Viewing the RMON History Table
- Configuring RMON Events
- Defining RMON Events Control
- Viewing the RMON Events Logs
- Defining RMON Alarms

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Amphenol Ruggedization Design

OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

TEMPERATURE:

- Operating Temperature- Thermal Cycles between -40ºC and 85ºC while device is operating
- Temperature is measured at chassis housing or card edge
- Storage Temperature- Thermal Cycles between -55ºC and 125ºC

HUMIDITY:

- Operating Humidity- Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity- Humidity cycle between 0-100% condensing humidity

SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION:

- Sine Vibration - 10g Peak, 5-2,000Hz
  - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
  - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
  - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

FLUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTRONMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
- Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL-HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

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