Amphenol
MILITARY HIGH SPEED

MEGA RUGGED ETHERNET SWITCH

432-CHANNEL 25G/100G Fiber Optic SWITCHBOX

Coming Soon—50G/400G Support!

DESCRIPTION

Amphenol's Rugged 432 Channel Ethernet Switch Box is liquid cooled and configurable for system connectivity, speeds, port types, and interoperation with various high-speed media converters and connectors for system interfacing.

The switch is manufactured using derivatives of Amphenol's MIL-DTL-38999 Series connectors. These connectors contain standard AS39029 qualified contacts and 48F MT Ferrule Fiber Optic contact assemblies. The MT ferrules are used for fiber optic Ethernet ports and the AS39029 style contacts are used for power inputs and management functions.

The switch comes with an intricate network management system that we call the Embedded Web System (EWS). The EWS configures, monitors, and troubleshoots network devices from a remote web browser. The EWS web pages are easy-to-use and easy-to-navigate. In addition, the EWS provides real time graphs and RMON statistics to help system administrators monitor network performance.

FEATURES & BENEFITS

- Chassis with 5x MT38999 Connectors to support either:
  - 432 25G Base SR Fiber - supports down to 1Gbps + any mix and match of 40G/100G Interfaces in x4 modes.
- 432 channels in total that can support up to 100G (x4) and 25G (x1) interfaces.
  - Complete NRZ support for 100G (x4), 50G (x2), 40G (x4), 25G (x1), 10G (x1) and 1G (x1) among others.
- Liquid cooling for rugged -40 - +85C environments
- Embedded Management system
  - Web and command line interface user guides.
- Supports Ethernet multicast, IP multicast, IGMP, SNMP, & many other management options.
- Host management processor
- Debug/Status connector & 270V DC power connector

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HOW TO ORDER

Part Number	CF-020400-054	432 Channels at 25G Max
	CF-020400-586	432 Channels at 25G Max
	CF-02WA00-24X	50G PAM-4 Support
	CF-02WA00-25X	50G PAM-4 Support

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SOFTWARE FEATURES

Stacking
Stacking Ring Topology
Stacking Chain Topology
Stacking Members and Unit ID
Removing and Replacing Stacking Members
Exchanging Stacking Members
Switching the Stacking Master
Configuring System Time
Configuring Daylight Savings Time
Configuring SNTP
Polling for Unicast Time Information
Polling for Anycast Time Information
Broadcast Time Information
Defining SNTP Settings
Configuring Device Security
Configuring Management Security
Configuring Authentication Methods
Defining Access Profiles
Defining Profile Rules
Defining Authentication Profiles
Mapping Authentication Methods
Defining RADIUS Settings
Defining TACACS+ Authentication
Configuring Passwords
Defining Local Users
Defining Line Passwords
Defining Enable Passwords
Configuring Network Security
Network Security Overview
Port-Based Authentication
Advanced Port-Based Authentication
Defining Port Authentication Properties
Defining Port Authentication
Configuring Multiple Hosts
Defining Authentication Hosts
Viewing EAP Statistics
Defining Access Control Lists
Defining IP Based Access Control Lists
Defining MAC Based Access Control Lists
Binding Device Security ACLs
Managing Port Security
Enabling Storm Control
Configuring System Logs
Defining General Log Properties
Viewing Memory Logs
Viewing Flash Logs
Defining System Log Servers
Configuring Interfaces
Configuring Ports
Aggregating Ports
Configuring LACP

Configuring VLANs
Defining VLAN Properties
Defining VLAN Membership
Defining VLAN Interface Settings
Configuring GARP
Defining GARP
Defining GVRP
Viewing GVRP Statistics
Defining IP Addresses
Configuring IP Addressing
Defining IP Addresses
Defining ARP
Defining Domain Name Servers
Defining DNS Servers
Defining DNS Host Mapping
Defining the Forwarding Database
Defining the Forwarding Database
Defining Access Profiles
Configuring Spanning Tree
Defining Classic Spanning Tree
Defining STP on Interfaces
Defining Rapid Spanning Tree
Defining Multiple Spanning Tree
Defining MSTP Instance Settings
Defining MSTP Interface Settings
Configuring SNMP
SNMP v1 and v2c
SNMP v3
Configuring SNMP Security
Defining SNMP Security
Defining SNMP View
Defining SNMP Group Profiles
Defining SNMP Group Members
Defining SNMP Communities
SNMP Communities Basic Table
SNMP Communities Advanced Table
Configuring SNMP Notifications
Defining SNMP Notification Global Parameters
Defining SNMP Notification Filters
Defining SNMP Notification Recipients
SNMPv1,2c Notification Recipients
SNMPv3 Notification Recipients
Configuring Multicast Forwarding
Multicast Forwarding
Typical Multicast Setup
Multicast Operation
Multicast Registration
Multicast Address Properties
Defining Multicast Properties
Adding MAC Group Address
Adding IP Multicast Groups

Configuring IGMP Snooping
Configuring MLD Snooping
Viewing IGMP/MLD IP Multicast Groups
Defining Multicast Router Ports
Defining Forward All Multicast
Defining Unregistered Multicast Settings
Managing System Files
Downloading System Files
Firmware Download
Configuration Download
Uploading System Files
Upload Type
Software Image Upload
Configuration Upload
Copying Files
Restoring the Default Configuration File
Configuring Quality of Service
Quality of Service Overview
VPT Classification Information
CoS Services
Defining General QoS Settings
Configuring QoS General Settings
Restoring Factory Default QoS Interface Settings
Defining Queues
Defining Bandwidth Settings
Mapping CoS Values to Queues
Mapping DSCP Values to Queues
Defining QoS Basic Mode
Defining Basic Mode Settings
Rewriting Basic Mode DSCP Values
Defining QoS Advanced Mode
Setting Policy Binding
Managing Device Diagnostics
Configuring Port Mirroring
Viewing Statistics
Viewing Interface Statistics
Viewing Interface Statistics
Receive Statistics
Transmit Statistics
Viewing Etherlike Statistics
Managing RMON Statistics
Viewing RMON Statistics
Configuring RMON History
Defining RMON History Control
Viewing the RMON History Table
Configuring RMON Events
Defining RMON Events Control
Viewing the RMON Events Logs
Defining RMON Alarms

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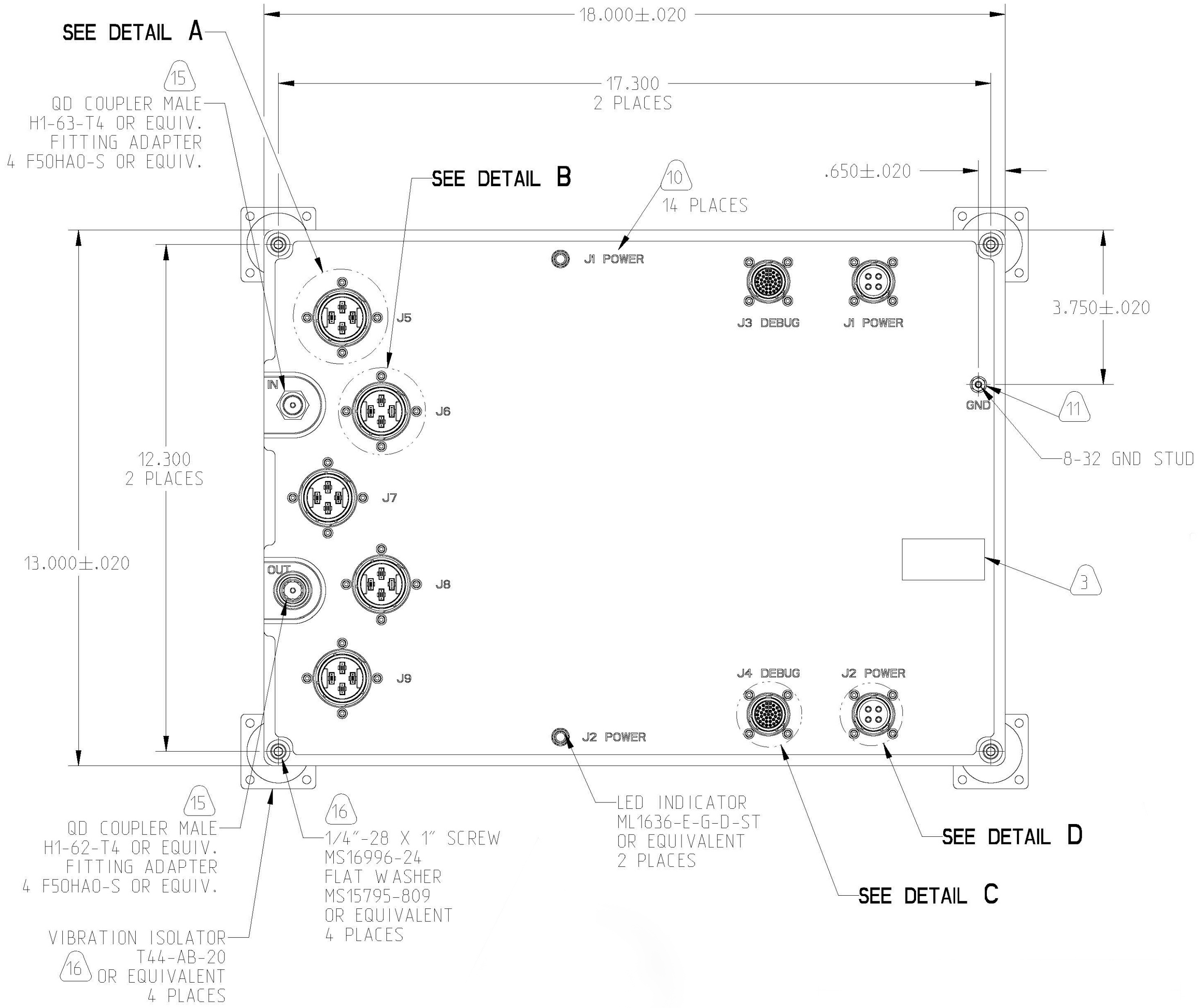
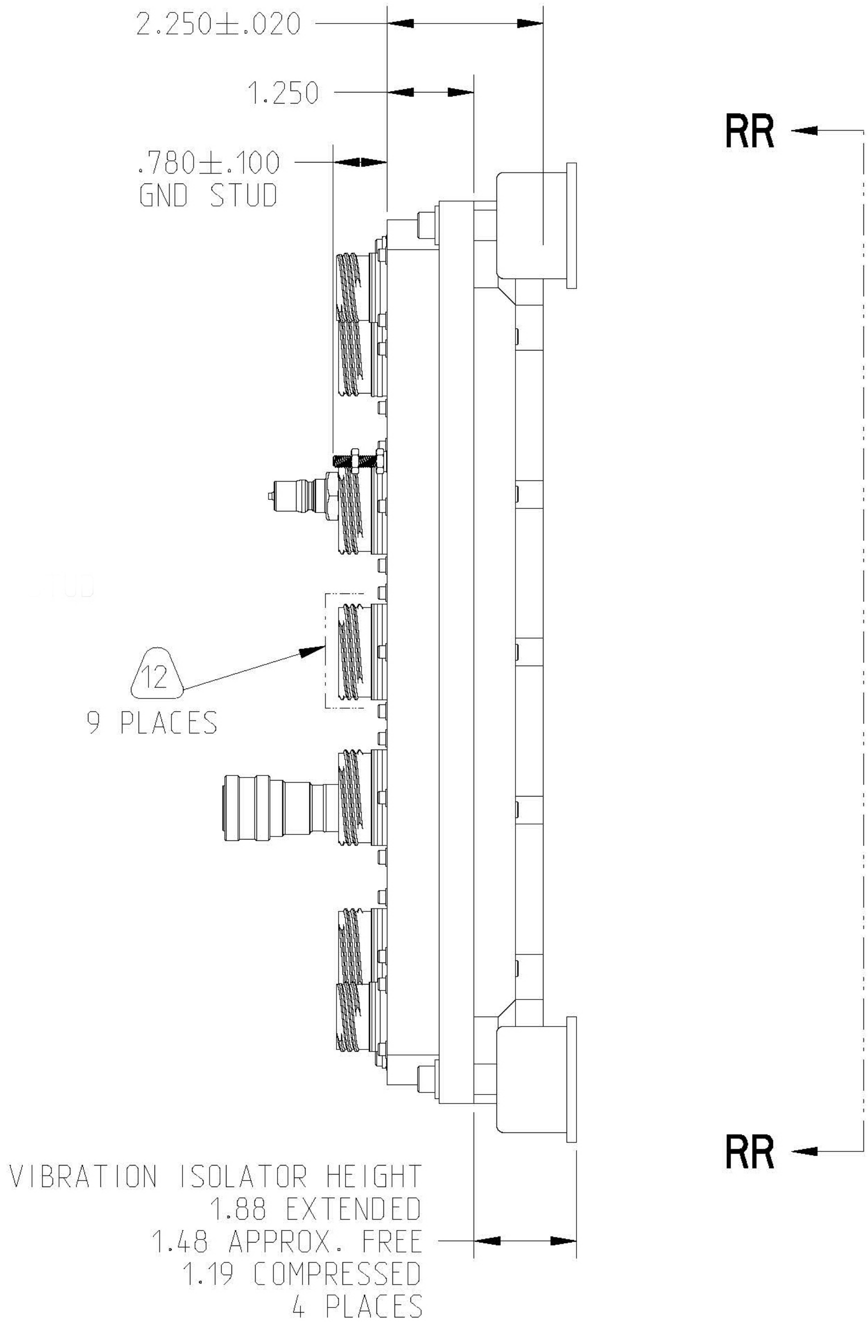
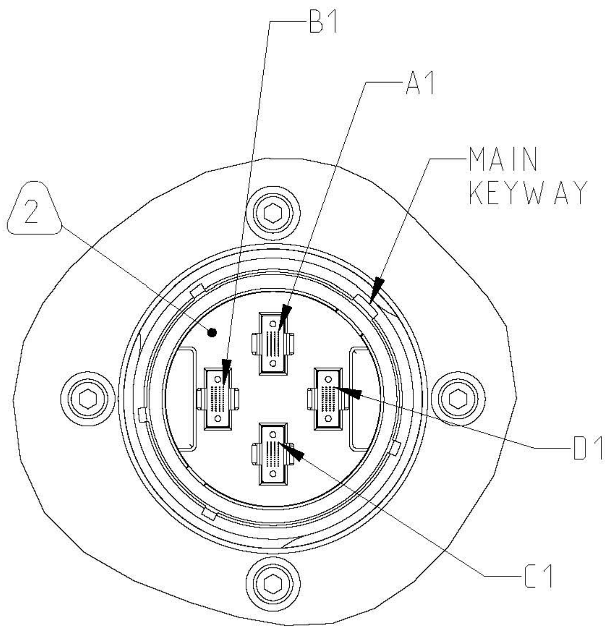
DIMENSIONAL INFORMATION (CF-020400-054)



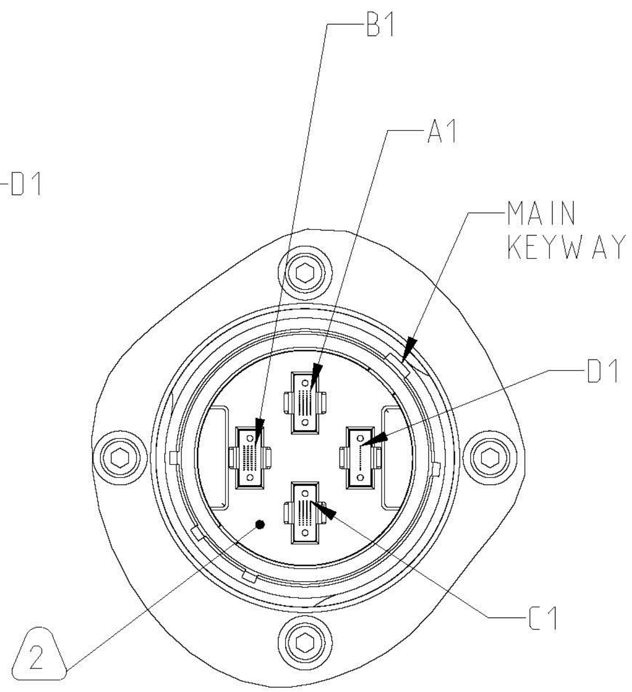
DIMENSIONAL INFORMATION (CF-020400-054, CONT.)



DIMENSIONAL INFORMATION (CF-020400-054, CONT.)

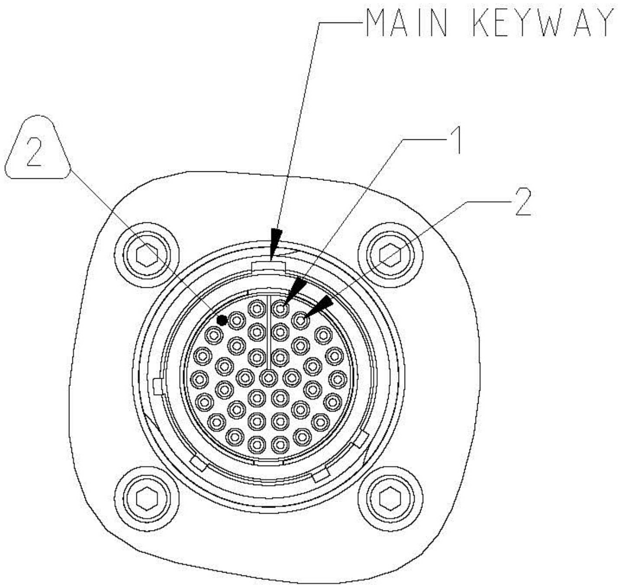


DETAIL A
J5, J7 AND J9
SCALE 1.500

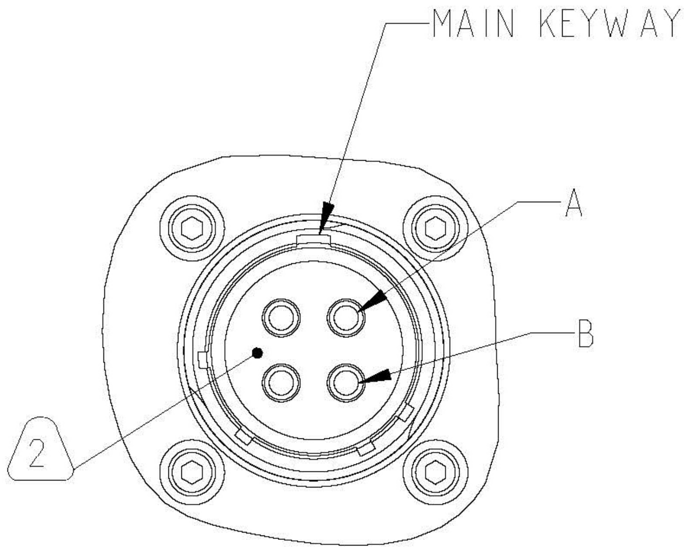


DETAIL B
J6 AND J8
SCALE 1.500

DIMENSIONAL INFORMATION (CF-020400-054, CONT.)



DETAIL C
J3 AND J4
SCALE 1.500



DETAIL D
J1 AND J2
SCALE 1.500

I/O Chart (CF-020400-054)

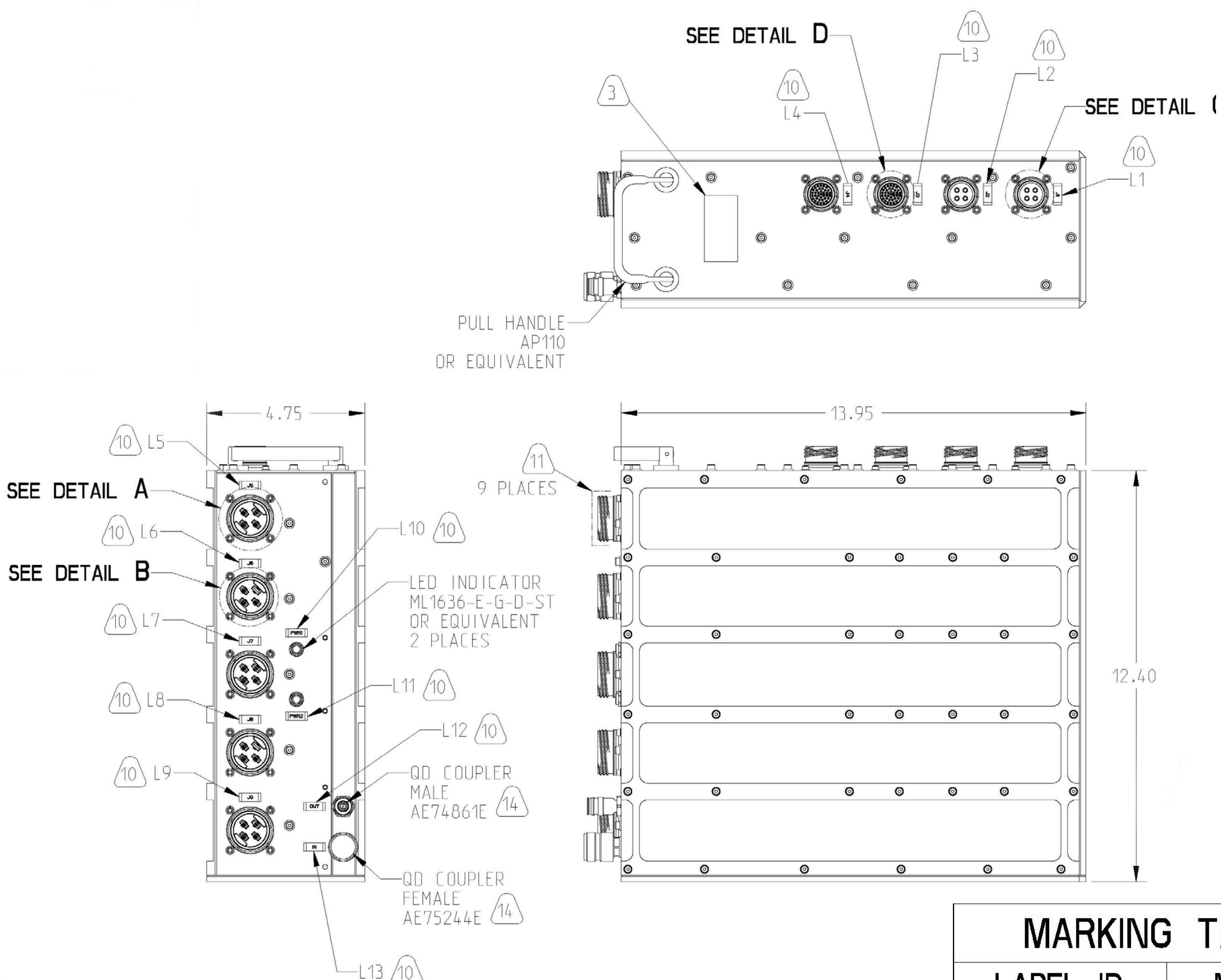
I/O CHART

CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	270VDC_IN
	B	OUT	270VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J3 (DEBUG) 15-35P KEYING "N"	1	OUT	CPU_RS232_CONSOLE_TX
	2	IN	CPU_RS232_CONSOLE_RX
	3	--	GND
	4	--	N/C
	5	--	N/C
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	N/C
	10	--	N/C
	11	--	GND
	12	BI	CPU_1GBase-T_DA+
	13		CPU_1GBase-T_DA-
	14		CPU_1GBase-T_DB+
	15		CPU_1GBase-T_DB-
	16		CPU_1GBase-T_DC+
	17		CPU_1GBase-T_DC-
	18		CPU_1GBase-T_DD+
	19		CPU_1GBase-T_DD-
	20	--	N/C
	21	--	GND
	22	--	N/C
	23	--	N/C
	24	--	N/C
	25	--	N/C
	26	--	N/C
	27	--	GND
	28	--	N/C
	29	--	N/C
	30	--	N/C
	31	--	N/C
	32	--	N/C
	33	--	N/C
	34	--	N/C
	35	--	N/C
	36	--	N/C
	37	--	N/C
	SHELL	--	CHASSIS

I/O CHART

CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 (POWER) 15-4P KEYING "N"	A	IN	270VDC_IN
	B	OUT	270VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J4 (DEBUG) 15-35P KEYING "N"	1	OUT	CPU_RS232_CONSOLE_TX
	2	IN	CPU_RS232_CONSOLE_RX
	3	--	GND
	4	--	N/C
	5	--	N/C
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	N/C
	10	--	N/C
	11	--	GND
	12	BI	CPU_1GBase-T_DA+
	13		CPU_1GBase-T_DA-
	14		CPU_1GBase-T_DB+
	15		CPU_1GBase-T_DB-
	16		CPU_1GBase-T_DC+
	17		CPU_1GBase-T_DC-
	18		CPU_1GBase-T_DD+
	19		CPU_1GBase-T_DD-
	20	--	N/C
	21	--	GND
	22	--	N/C
	23	--	N/C
	24	--	N/C
	25	--	N/C
	26	--	N/C
	27	--	GND
	28	--	N/C
	29	--	N/C
	30	--	N/C
	31	--	N/C
	32	--	N/C
	33	--	N/C
	34	--	N/C
	35	--	N/C
	36	--	N/C
	37	--	N/C
	SHELL	--	CHASSIS

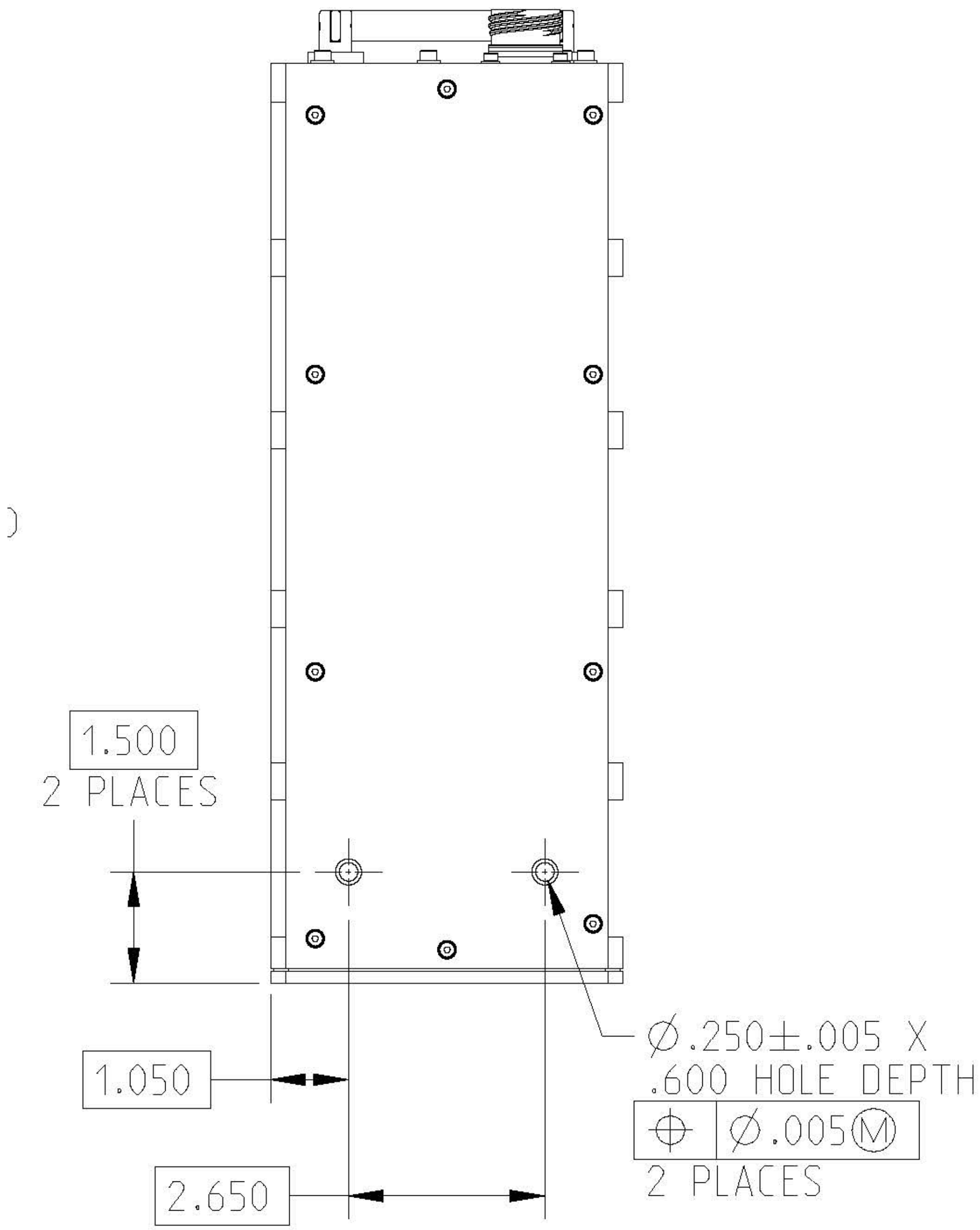
DIMENSIONAL INFORMATION (CF-020400-586)



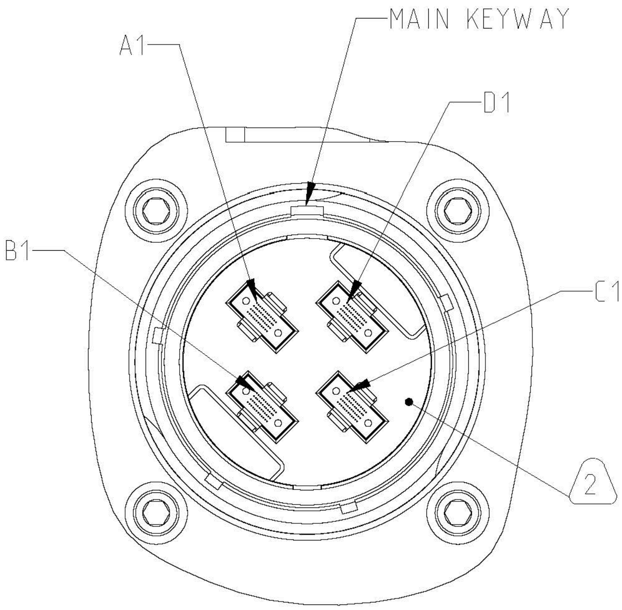
MARKING TABLE 10

LABEL ID	MARKING
L1	J1
L2	J2
L3	J3
L4	J4
L5	J5
L6	J6
L7	J7
L8	J8
L9	J9
L10	PWR1
L11	PWR2
L12	OUT
L13	IN

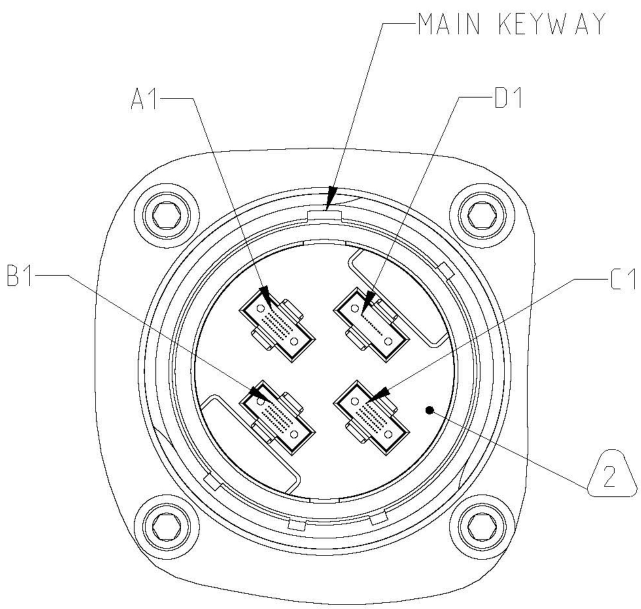
DIMENSIONAL INFORMATION (CF-020400-586, CONT.)



DIMENSIONAL INFORMATION (CF-020400-586, CONT.)

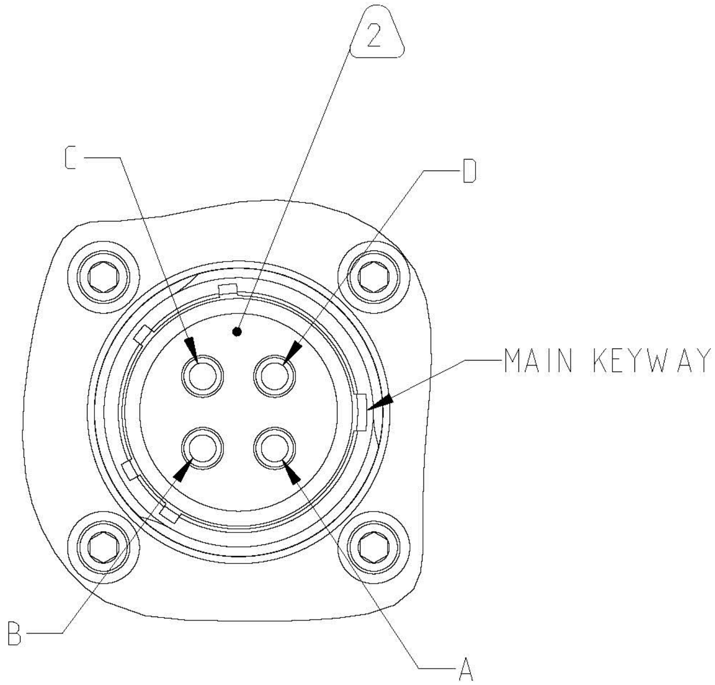


DETAIL A
J5, J7 AND J9
SCALE 2.000

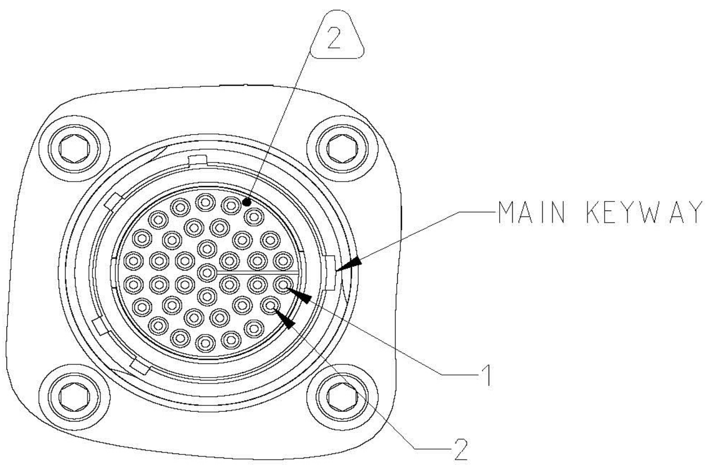


DETAIL B
J6 AND J8
SCALE 2.000

DIMENSIONAL INFORMATION (CF-020400-586, CONT.)



DETAIL C
J1 AND J2
SCALE 2.000



DETAIL D
J3 AND J4
SCALE 2.000

I/O Chart (CF-020400-586)

I/O CHART

CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	270VDC_IN
	B	OUT	270VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J3 (DEBUG) 15-35P KEYING "N"	1	OUT	CPU_RS232_CONSOLE_TX
	2	IN	CPU_RS232_CONSOLE_RX
	3	--	GND
	4	--	N/C
	5	--	N/C
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	N/C
	10	--	N/C
	11	--	GND
	12	BI	CPU_1GBase-T_DA+
	13		CPU_1GBase-T_DA-
	14		CPU_1GBase-T_DB+
	15		CPU_1GBase-T_DB-
	16		CPU_1GBase-T_DC+
	17		CPU_1GBase-T_DC-
	18		CPU_1GBase-T_DD+
	19		CPU_1GBase-T_DD-
	20	--	N/C
	21	--	GND
	22	--	N/C
	23	--	N/C
	24	--	N/C
	25	--	N/C
	26	--	N/C
	27	--	GND
	28	--	N/C
	29	--	N/C
	30	--	N/C
	31	--	N/C
	32	--	N/C
	33	--	N/C
	34	--	N/C
	35	--	N/C
	36	--	N/C
	37	--	N/C
	SHELL	--	CHASSIS

I/O CHART

CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 (POWER) 15-4P KEYING "N"	A	IN	270VDC_IN
	B	OUT	270VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J4 (DEBUG) 15-35P KEYING "N"	1	OUT	CPU_RS232_CONSOLE_TX
	2	IN	CPU_RS232_CONSOLE_RX
	3	--	GND
	4	--	N/C
	5	--	N/C
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	N/C
	10	--	N/C
	11	--	GND
	12	BI	CPU_1GBase-T_DA+
	13		CPU_1GBase-T_DA-
	14		CPU_1GBase-T_DB+
	15		CPU_1GBase-T_DB-
	16		CPU_1GBase-T_DC+
	17		CPU_1GBase-T_DC-
	18		CPU_1GBase-T_DD+
	19		CPU_1GBase-T_DD-
	20	--	N/C
	21	--	GND
	22	--	N/C
	23	--	N/C
	24	--	N/C
	25	--	N/C
	26	--	N/C
	27	--	GND
	28	--	N/C
	29	--	N/C
	30	--	N/C
	31	--	N/C
	32	--	N/C
	33	--	N/C
	34	--	N/C
	35	--	N/C
	36	--	N/C
	37	--	N/C
	SHELL	--	CHASSIS

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Amphenol Ruggedization Design

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OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

TEMPERATURE:

- Operating Temperature- Thermal Cycles between -40°C and 85°C while device is operating
- Temperature is measured at chassis housing or card edge
- Storage Temperature- Thermal Cycles between -55°C and 125°C

HUMIDITY:

- Operating Humidity- Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity- Humidity cycle between 0-100% condensing humidity

SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION:

- Sine Vibration - 10g Peak, 5-2,000Hz
    - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
    - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
    - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

FLUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTRONMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
- Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL- HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

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