DIGITAL COMMAND CENTER

Family of multi-channel Standalone Network Switches

The Tactician

The General

The Architect

DESCRIPTION:

Amphenol's family of Rugged Digital Command Center Ethernet Switch Boxes provides an unmatched level of flexibility to meet any system requirement. The base model switch box is a 32-channel 10Gbps standalone Ethernet Switch box that is configurable for system connectivity, speeds, port types, and interoperation with various high-speed media converters and connectors for system interfacing. In addition, each switch is non-blocking and low-latency for high-throughput architectures and applications. In Amphenol's state-of-the-art Spirent communications testing center, the switch box is tested aggressively at line rates to RFC 2889 for switching and RFC 2544 for L2/L3 performance, latency, packet forwarding, and other key items at full line rate and PRBS 2^{31}.

The **Pro Light** comprises of 12 channels of 10GBASE-T (supporting 1GBASE-T and 100BASE-T), and four channels of 10GBASE-SR, capable of a throughput of up to 160Gbps.

Need more channels? Check out the **Pro Performance** model that can support 24 channels of 10GBASE-T (supporting 1GBASE-T and 100BASE-T), and eight channels of 10GBASE-SR.

Everyone needs to go faster eventually! Check out the **Pro 25G** version which has eight channels of 10GBASE-T and 24 channels of 25GBASE-SR utilizing state of the art fiber optic transceivers.

FEATURES AND BENEFITS:

- Copper Ethernet compliance to IEEE 802.3an
- Fiber Ethernet compliant to IEEE 802.3 Clause 49
- Non-blocking L2/L3 switch
- Dual core ARM processor with flash, SPI, EEPROMs, and DDR3 and management Ethernet connection
- Uboot and Linux OS for L2/L3 switching
- Web browser, SSH, CLI, telnet
- Embedded reset and status CPLD
- Support for PTP boundary clock
- Service micro-controller for power down, reset, and restart in overheat event
- 28VDC mil-spec power supply with EMI filter
- ETI, Circuit breaker, power supply status LEDs
- Power connector, debug connector, maintenance/ status connector - MIL-STD-38999
- MIL spec black painted chassis with cold plate and external conduction cooling
- Power over Ethernet (POE) on select units
- MIL spec circuit breaker

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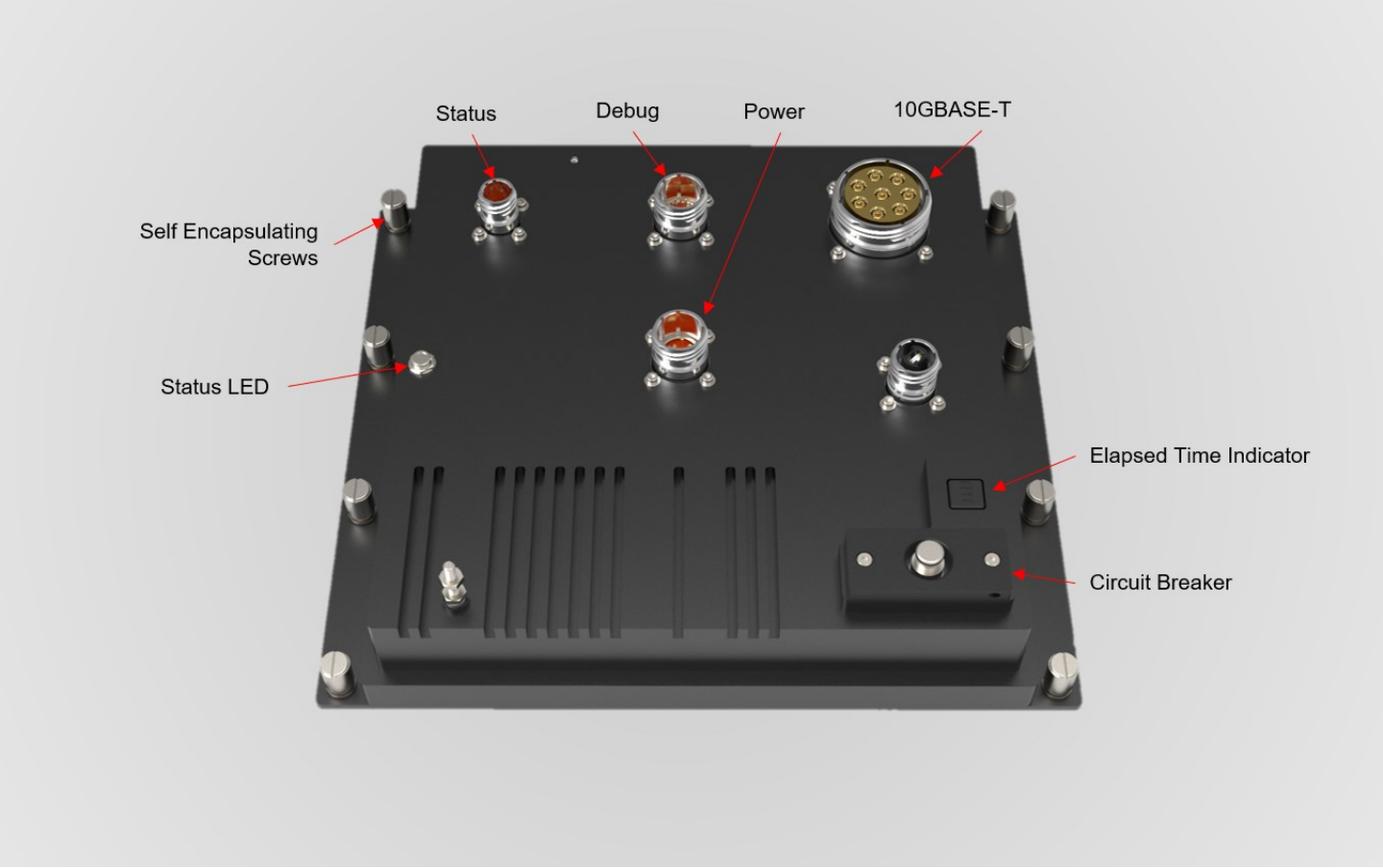
ORDERING INFORMATION

PART NUMBER	ALIAS	10GBASE-T CHANNELS	10GBASE-SR CHANNELS	25GBASE-SR CHANNELS	POE
CF-02WA00-042	The Architect	12	4	0	Yes
CF-02WA00-041	The Tactician	24	8		Yes
CF-020400-062	The General	8	0*	24	No
CF-02WA00-12X	The Sargent	36	0*	12	No
CF-02WA00-13X	The Specialist	25	0*	12	No
CF-02WA00-14X	The Private	12	0*	12	No

*25GBASE-SR channels support 10GBASE-SR

VISUAL DESCRIPTION



Functionality differs based on Digital Command Center model

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Software Features

Stacking
Stacking Ring Topology
Stacking Chain Topology
Stacking Members and Unit ID
Removing and Replacing Stacking Members
Exchanging Stacking Members
Switching the Stacking Master
Configuring System Time
Configuring Daylight Savings Time
Configuring SNTP
Polling for Unicast Time Information
Polling for Anycast Time Information
Broadcast Time Information
Defining SNTP Settings
Configuring Device Security
Configuring Management Security
Configuring Authentication Methods
Defining Access Profiles
Defining Profile Rules
Defining Authentication Profiles
Mapping Authentication Methods
Defining RADIUS Settings
Defining TACACS+ Authentication
Configuring Passwords
Defining Local Users
Defining Line Passwords
Defining Enable Passwords
Configuring Network Security
Network Security Overview
Port-Based Authentication
Advanced Port-Based Authentication
Defining Port Authentication Properties
Defining Port Authentication
Configuring Multiple Hosts
Defining Authentication Hosts
Viewing EAP Statistics
Defining Access Control Lists
Defining IP Based Access Control Lists
Defining MAC Based Access Control Lists
Binding Device Security ACLs
Managing Port Security
Enabling Storm Control
Configuring System Logs
Defining General Log Properties
Viewing Memory Logs
Viewing Flash Logs
Configuring Interfaces
Configuring Ports
Aggregating Ports
Configuring LACP
Configuring VLANs
Defining VLAN Properties
Defining VLAN Membership
Defining VLAN Interface Settings
Configuring GARP
Defining GARP
Defining GVRP
Viewing GVRP Statistics

Defining IP Addresses
Configuring IP Addressing
Defining IP Addresses
Defining ARP
Defining Domain Name Servers
Defining DNS Servers
Defining DNS Host Mapping
Defining the Forwarding Database
Defining Static Forwarding Database Entries
Defining Dynamic Forwarding Database Entries
Configuring Spanning Tree
Defining Classic Spanning Tree
Defining STP on Interfaces
Defining Rapid Spanning Tree
Defining Multiple Spanning Tree
Defining MSTP Instance Settings
Defining MSTP Interface Settings
Configuring SNMP
SNMP v1 and v2c
SNMP v3
Configuring SNMP Security
Defining SNMP Security
Defining SNMP View
Defining SNMP Group Profiles
Defining SNMP Group Members
Defining SNMP Communities
SNMP Communities Basic Table
SNMP Communities Advanced Table
Configuring SNMP Notifications
Defining SNMP Notification Global Parameters .
Defining SNMP Notification Filters
Defining SNMP Notification Recipients
SNMPv1,2c Notification Recipients
SNMPv3 Notification Recipients
Configuring Multicast Forwarding
Multicast Forwarding
Typical Multicast Setup
Multicast Operation
Multicast Registration
Multicast Address Properties
Defining Multicast Properties
Adding MAC Group Address
Adding IP Multicast Groups
Configuring IGMP Snooping
Configuring MLD Snooping
Viewing IGMP/MLD IP Multicast Groups
Defining Multicast Router Ports
Defining Forward All Multicast
Defining Unregistered Multicast Settings

Managing System Files
Downloading System Files
Firmware Download
Configuration Download
Uploading System Files
Upload Type
Software Image Upload
Configuration Upload
Copying Files
Restoring the Default Configuration File
Configuring Quality of Service
Quality of Service Overview
VPT Classification Information
CoS Services
Defining General QoS Settings
Configuring QoS General Settings
Restoring Factory Default QoS Interface Settings
Defining Queues
Defining Bandwidth Settings
Mapping CoS Values to Queues
Mapping DSCP Values to Queues
Defining QoS Basic Mode
Defining Basic Mode Settings
Rewriting Basic Mode DSCP Values
Defining QoS Advanced Mode
Setting Policy Binding
Managing Device Diagnostics
Configuring Port Mirroring
Viewing Statistics
Viewing Interface Statistics
Viewing Interface Statistics
Receive Statistics
Transmit Statistics
Viewing Etherlike Statistics
Managing RMON Statistics
Viewing RMON Statistics
Configuring RMON History
Defining RMON History Control
Viewing the RMON History Table
Configuring RMON Events
Defining RMON Events Control
Viewing the RMON Events Logs
Defining RMON Alarms

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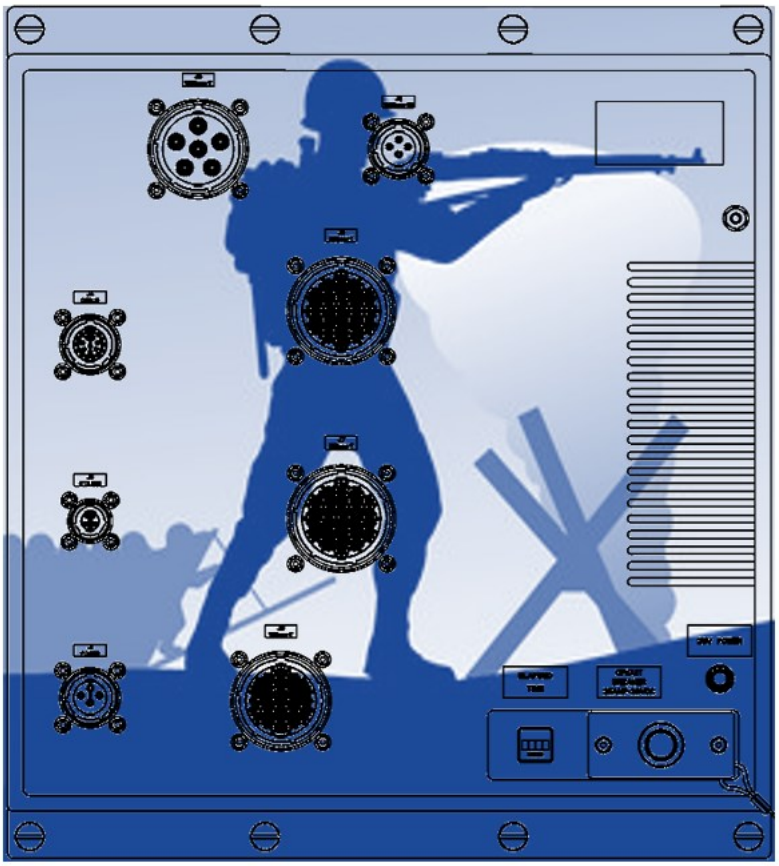
DIGITAL COMMAND CENTER

Our switches will be breaching the enemy lines in the battle! We will storm through the beaches of the market and onto the lovely land of victory with our "Digital Command Center".



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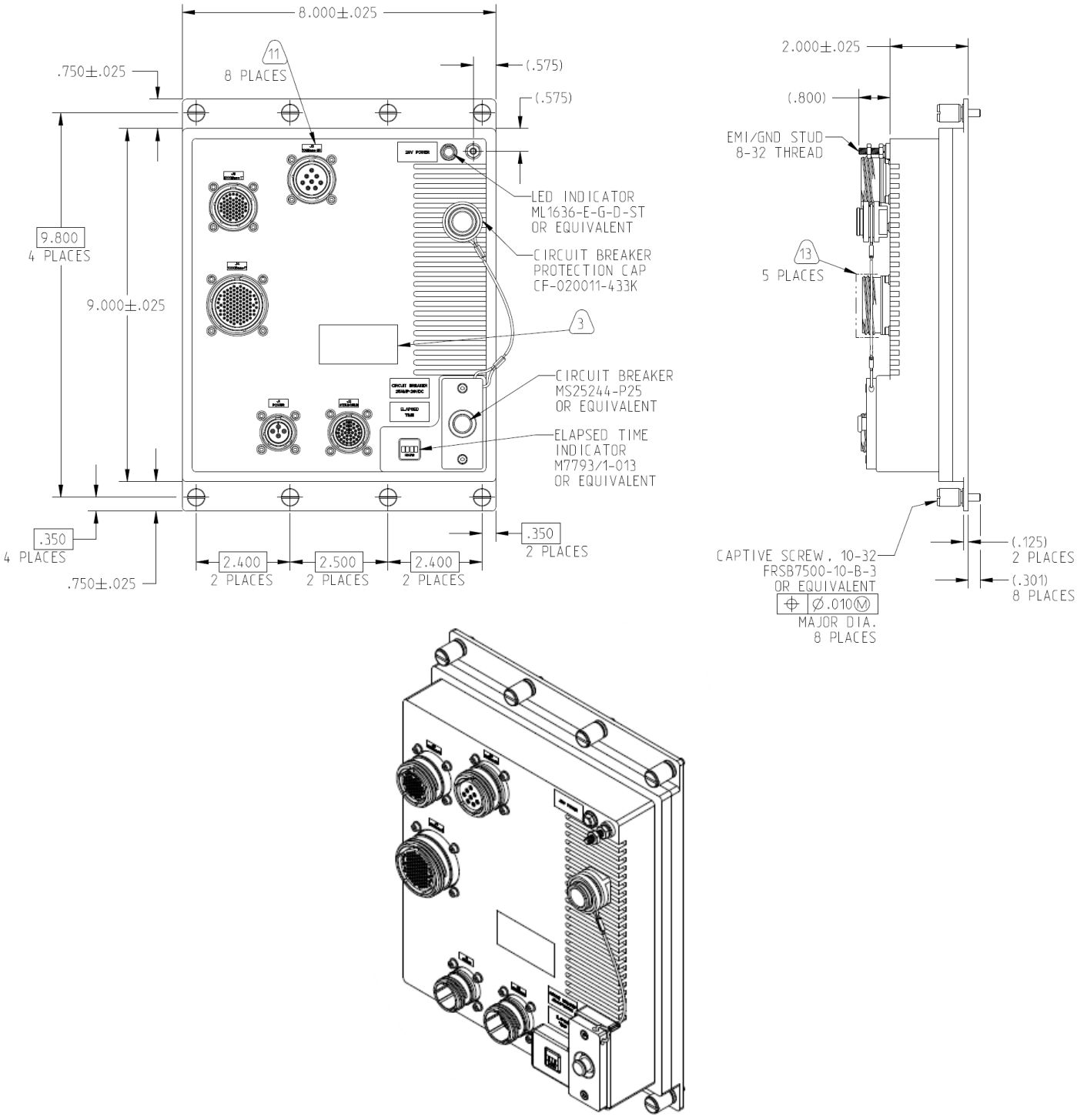
MECHANICAL SPECIFICATIONS

CF-02WA00-042 – Digital Command Center – The Architect



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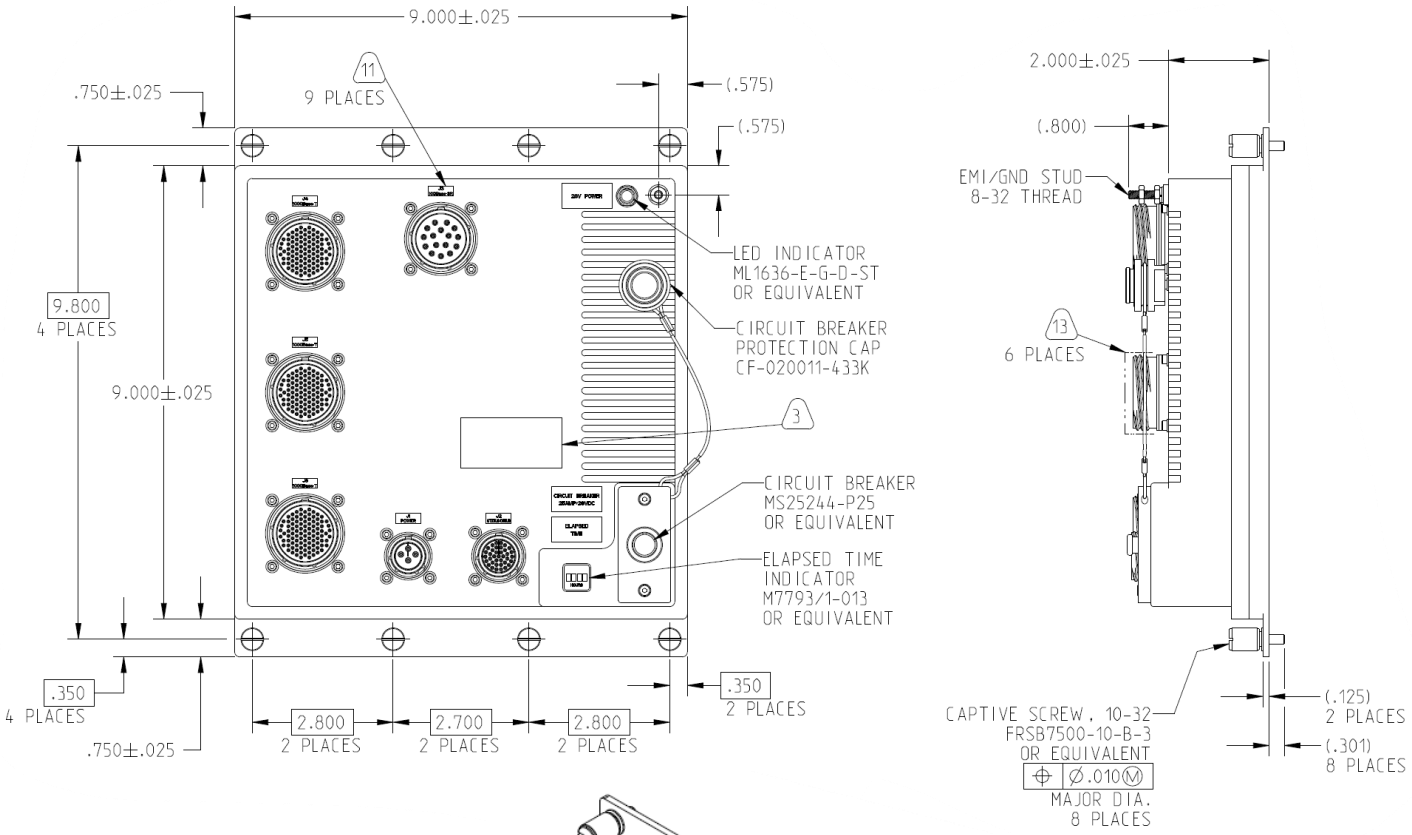
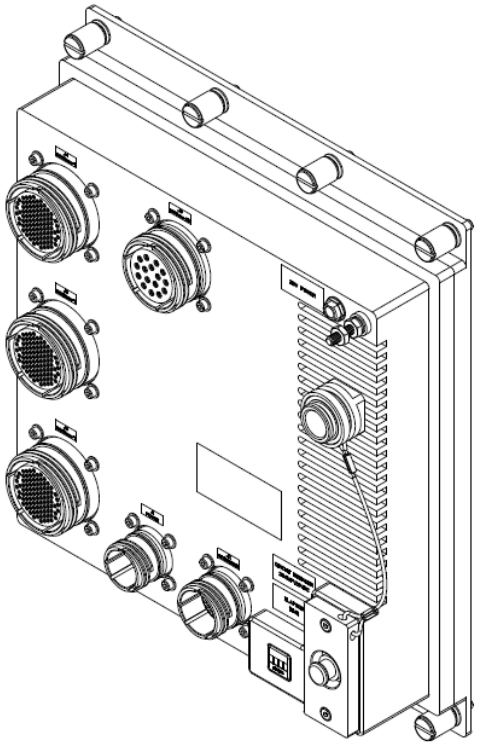
CF-02WA00-041 - Digital Command Center – The Tactician





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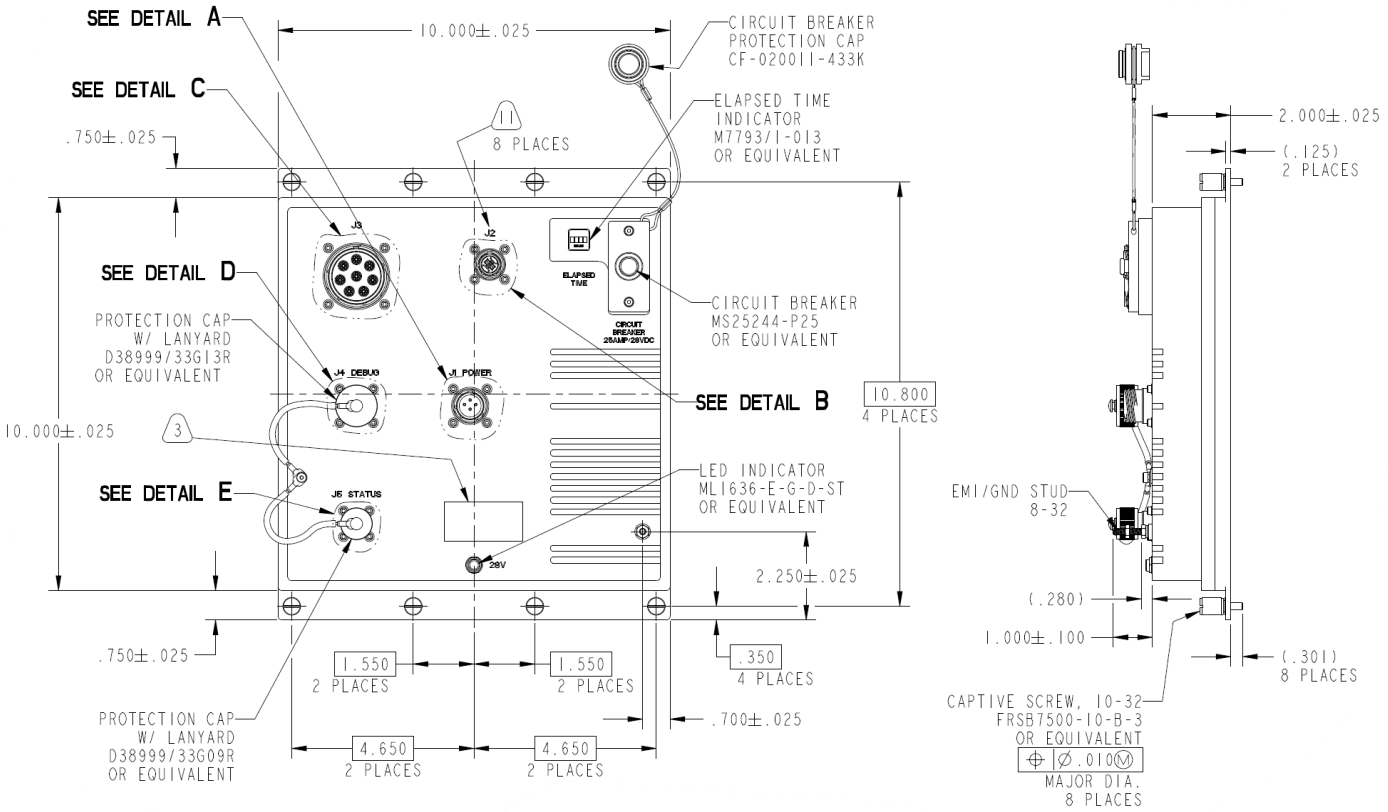
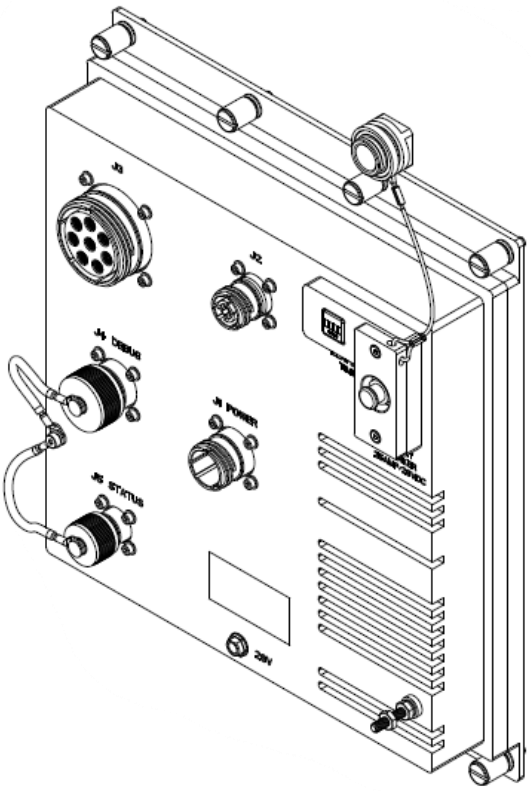
CF-020400-062 – Digital Command Center – The General





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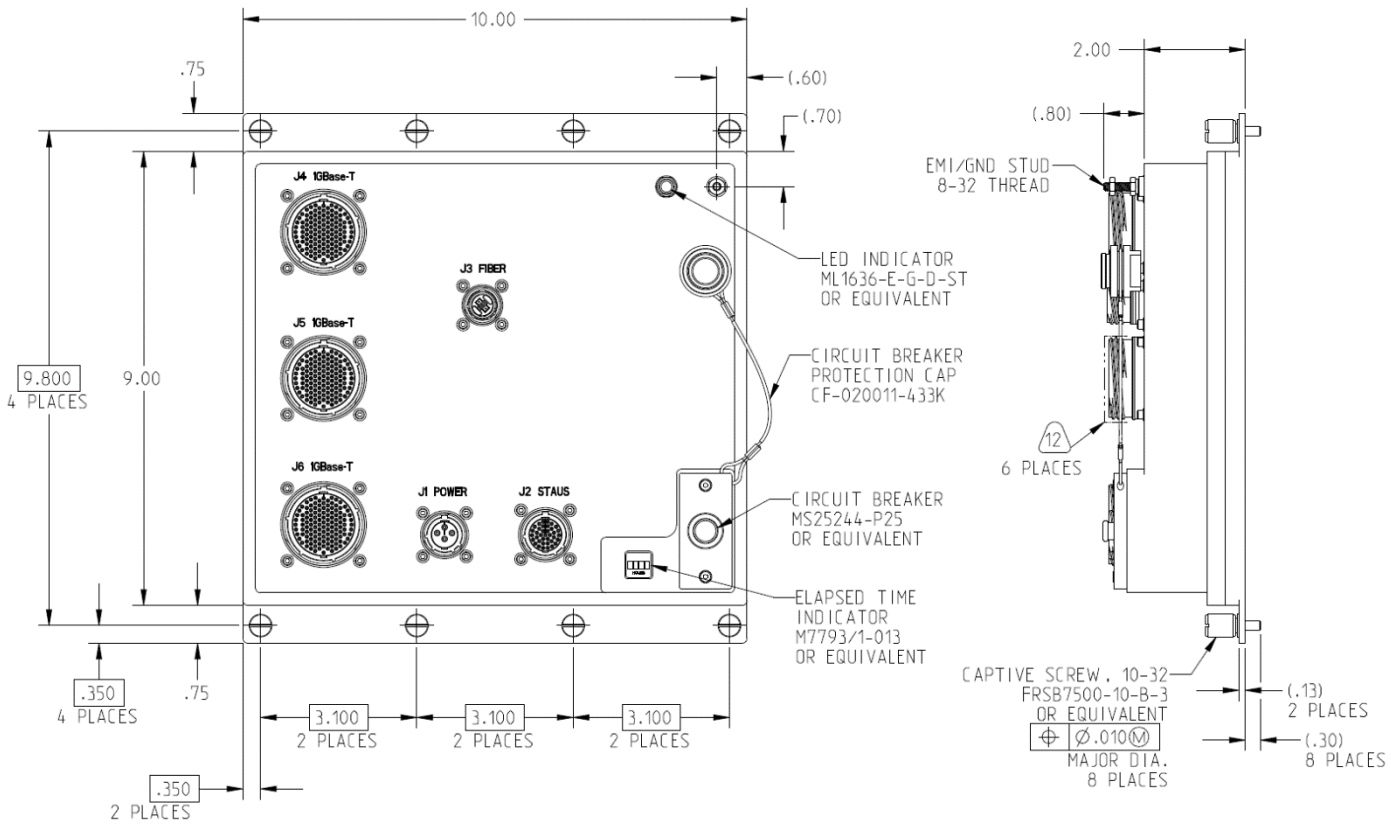
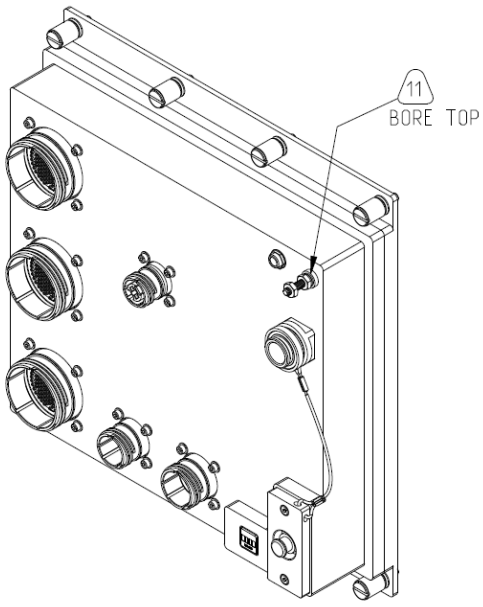
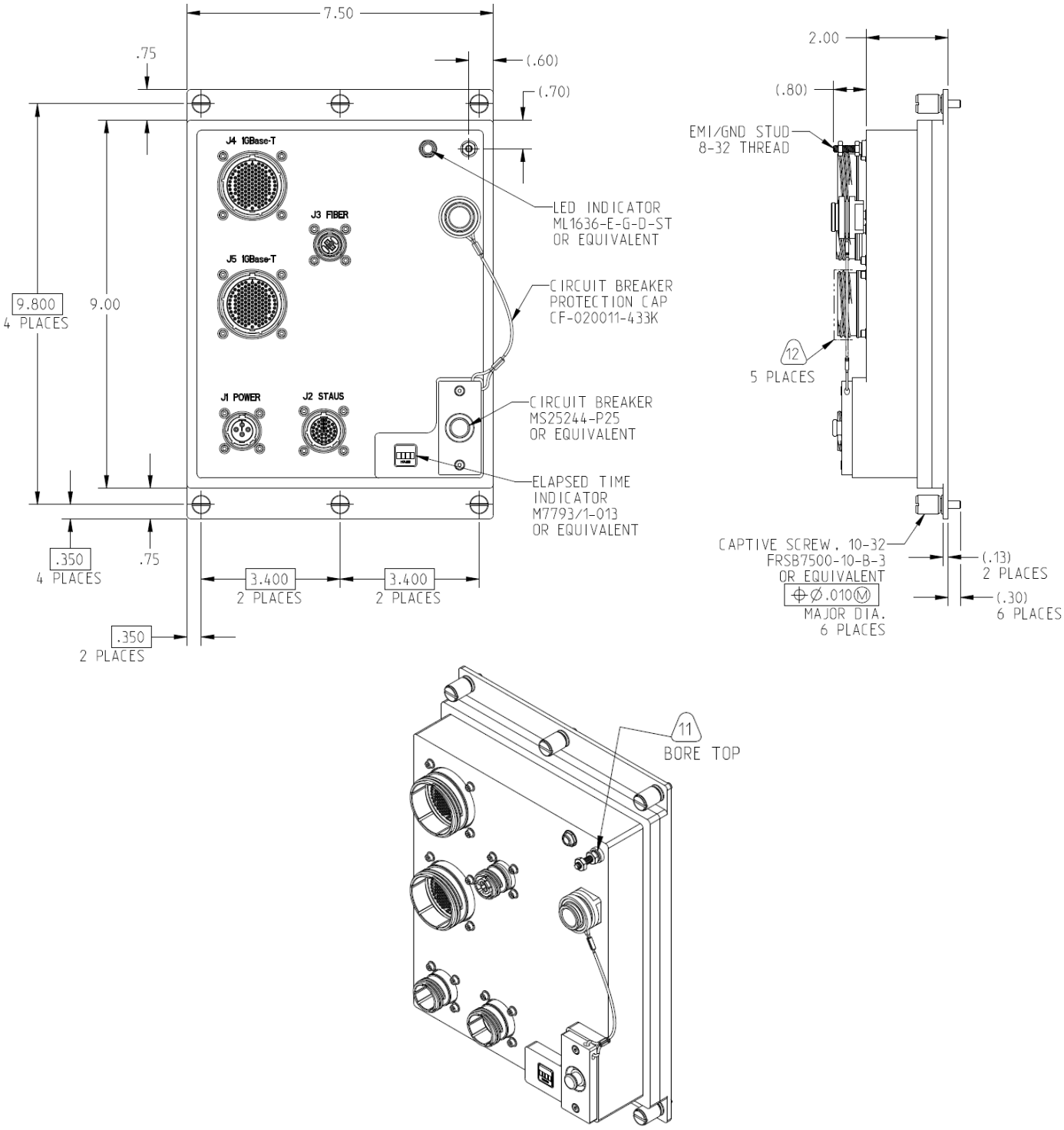
CF-02WA00-12X – Digital Command Center – The Sergent





CF-02WA00-13X – Digital Command Center – **The Specialist**



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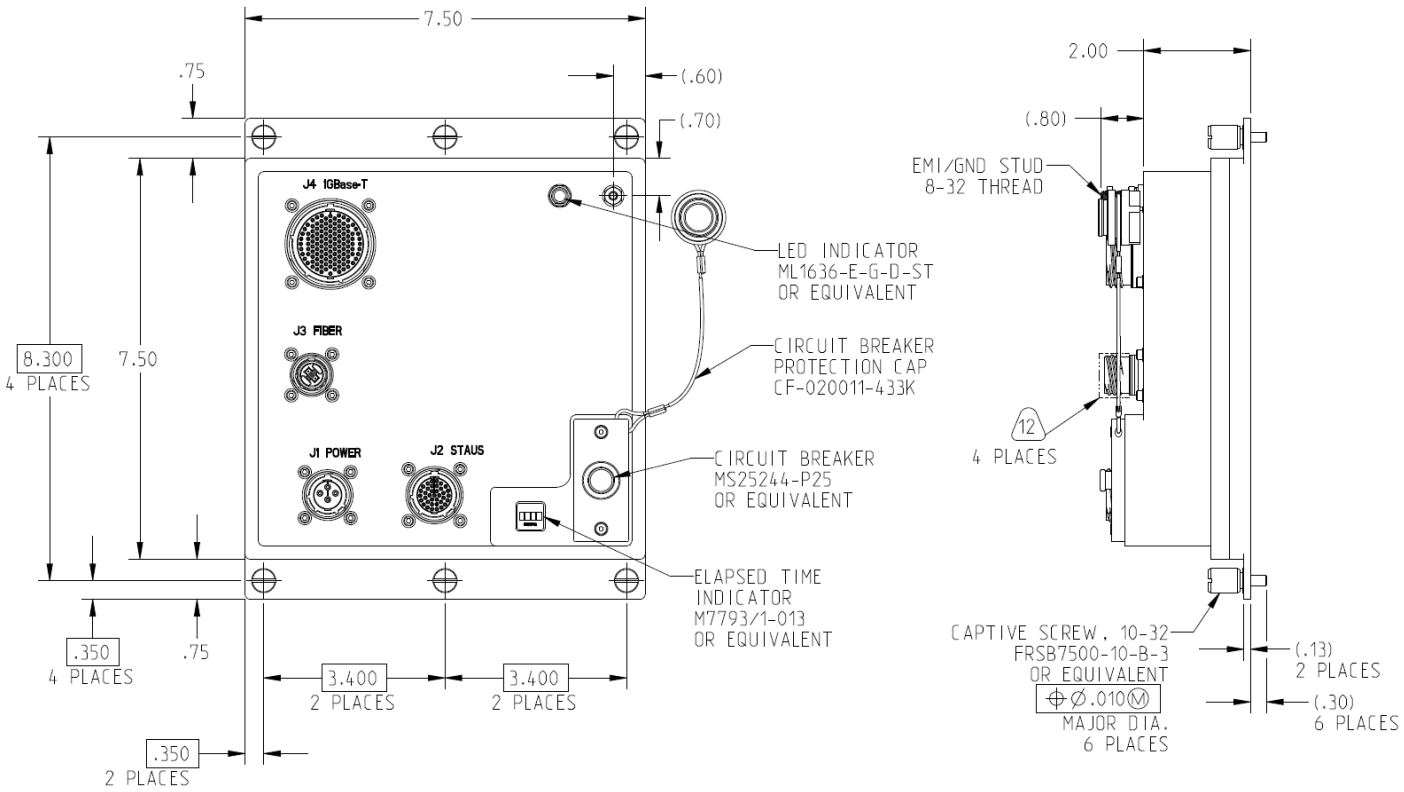
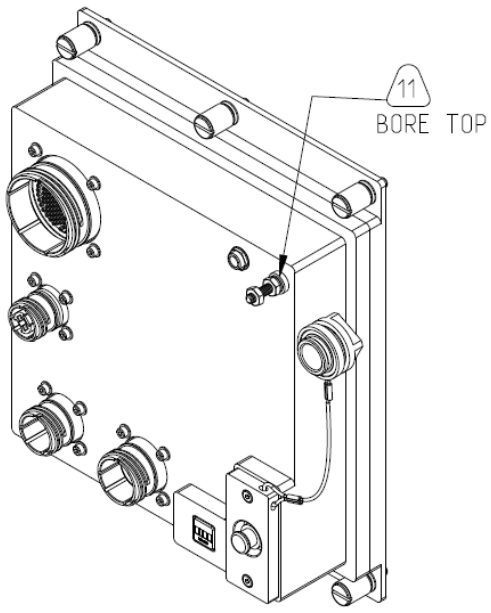
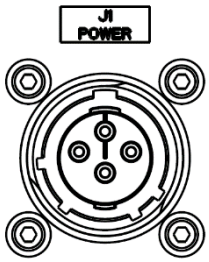
CF-02WA00-14X – Digital Command Center – **The Private**

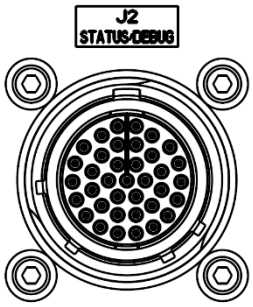




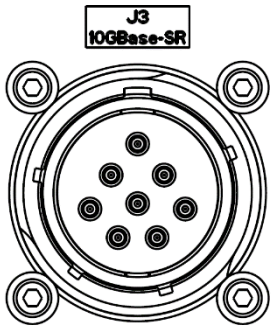
PINOUT – Digital Command Center The Architect

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 13-4P KEYING “N”	A	IN	280VDC_IN
	B	OUT	28VDC_RTN
	C	---	SAFETY GROUND / CHASSIS
	D	---	NOT CONNECTED
	SHELL	---	CHASSIS
J2 (DEBUG/ STATUS) 15-35P KEYING “N”	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	--	DEBUG_I2C_SCL
	5	--	DEBUG_I2C_SDA
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	MDIO_DATA
	10	--	MDIO_CLOCK
	11	--	GND
	12	BI	DEBUG_CPU_1GBASET_DA+
	13		DEBUG_CPU_1GBASET_DA-
	14		DEBUG_CPU_1GBASET_DB+
	15		DEBUG_CPU_1GBASET_DB-
	16		DEBUG_CPU_1GBASET_DC+
	17		DEBUG_CPU_1GBASET_DC-
	18		DEBUG_CPU_1GBASET_DD+
	19		DEBUG_CPU_1GBASET_DD-
	20	--	PIC_PROG_3.3V
	21	--	GND
	22	--	PIC_PROG_PGC
	23	--	PIC_PROG_MCLR
	24	--	PIC_PROG_PGD
	25	--	PIC_RS232_CONSOLE_TX
	26	--	PIC_RS232_CONSOLE_RX
	27	--	GND
	28-37	--	NOT CONNECTED
	SHELL	--	CHASSIS



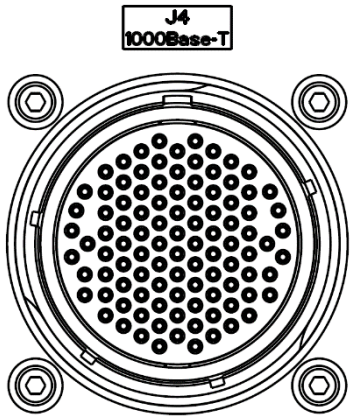


I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J3 10GBASE-SR 17-8S KEYING “N”	A	OUT	10GBASE-SR_TX	1
	B	IN	10GBASE-SR_RX	
	C	OUT	10GBASE-SR_TX	2
	D	IN	10GBASE-SR_RX	
	E	OUT	10GBASE-SR_TX	3
	F	IN	10GBASE-SR_RX	
	G	OUT	10GBASE-SR_TX	4
	H	IN	10GBASE-SR_RX	
	SHELL	---	CHASSIS	



PINOUT - Digital Command Center The Architect

I/O CHART								
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J4 10GBASE-T 23-35S KEYING “N”	1	BI	10GBASE-T_DA+	5	51	BI	10GBASE-T_DA+	10
	8		10GBASE-T_DA-		52		10GBASE-T_DA-	
	9		10GBASE-T_DB+		54		10GBASE-T_DB+	
	16		10GBASE-T_DB-		55		10GBASE-T_DB-	
	25		10GBASE-T_DC+		61		10GBASE-T_DC+	
	35		10GBASE-T_DC-		62		10GBASE-T_DC-	
	36		10GBASE-T_DD+		64		10GBASE-T_DD+	
	46		10GBASE-T_DD-		65		10GBASE-T_DD-	
	2	BI	10GBASE-T_DA+	6	77	BI	10GBASE-T_DA+	11
	3		10GBASE-T_DA-		78		10GBASE-T_DA-	
	5		10GBASE-T_DB+		79		10GBASE-T_DB+	
	6		10GBASE-T_DB-		80		10GBASE-T_DB-	
	11		10GBASE-T_DC+		81		10GBASE-T_DC+	
	12		10GBASE-T_DC-		89		10GBASE-T_DC-	
	14		10GBASE-T_DD+		87		10GBASE-T_DD+	
	15		10GBASE-T_DD-		88		10GBASE-T_DD-	
	18	BI	10GBASE-T_DA+	7	82	BI	10GBASE-T_DA+	12
	19		10GBASE-T_DA-		83		10GBASE-T_DA-	
	20		10GBASE-T_DB+		4		10GBASE-T_DB+	
	21		10GBASE-T_DB-		93		10GBASE-T_DB-	
	22		10GBASE-T_DC+		91		10GBASE-T_DC+	
	23		10GBASE-T_DC-		97		10GBASE-T_DC-	
	33		10GBASE-T_DD+		99		10GBASE-T_DD+	
	34		10GBASE-T_DD-		100		10GBASE-T_DD-	
	27	BI	10GBASE-T_DA+	8	50, 74, 75, 98	--	SPARE	--
	37		10GBASE-T_DA-		Rest	--	GND	--
	39		10GBASE-T_DB+					
	40		10GBASE-T_DB-					
	42		10GBASE-T_DC+					
	43		10GBASE-T_DC-					
	48		10GBASE-T_DD+					
	49		10GBASE-T_DD-					
	51	BI	10GBASE-T_DA+	7				
	52		10GBASE-T_DA-					
	54		10GBASE-T_DB+					
	55		10GBASE-T_DB-					
	61		10GBASE-T_DC+					
	62		10GBASE-T_DC-					
	64		10GBASE-T_DD+					
	65		10GBASE-T_DD-					



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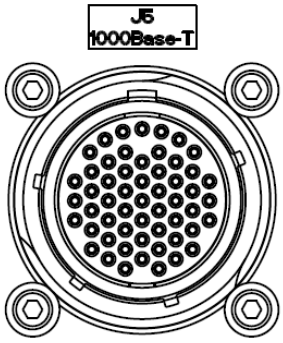
PINOUT - Digital Command Center The Architect

I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J5 10GBASE-T 17-35S KEYING "N"	1	BI	10GBASE-T_DA+	13
	6		10GBASE-T_DA-	
	2		10GBASE-T_DB+	
	7		10GBASE-T_DB-	
	3		10GBASE-T_DC+	
	8		10GBASE-T_DC-	
	4		10GBASE-T_DD+	
	5		10GBASE-T_DD-	
	17	BI	10GBASE-T_DA+	14
	18		10GBASE-T_DA-	
	19		10GBASE-T_DB+	
	20		10GBASE-T_DB-	
	21		10GBASE-T_DC+	
	22		10GBASE-T_DC-	
	23		10GBASE-T_DD+	
	24		10GBASE-T_DD-	
	3	BI	10GBASE-T_DA+	15
	33		10GBASE-T_DA-	
	34		10GBASE-T_DB+	
	35		10GBASE-T_DB-	
	36		10GBASE-T_DC+	
	37		10GBASE-T_DC-	
	38		10GBASE-T_DD+	
	39		10GBASE-T_DD-	
	48	BI	10GBASE-T_DA+	16
	53		10GBASE-T_DA-	
	59		10GBASE-T_DB+	
	54		10GBASE-T_DB-	
	50		10GBASE-T_DC+	
	55		10GBASE-T_DC-	
	51		10GBASE-T_DD+	
	52		10GBASE-T_DD-	
	9	--	SPARE	--
	47			
	Rest	--	GND	--

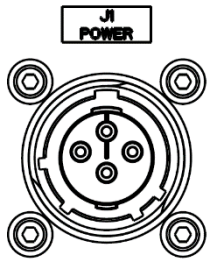


CONNECTOR LIST - Digital Command Center The Architect

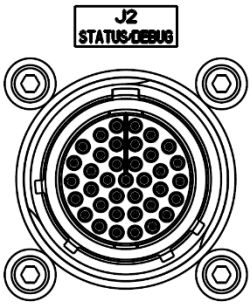
CONNECTOR LIST				
CONNECTOR DESIGNATOR	CONNECTOR PART NUMBER	CONTACT(S) USED	MATING CONNECTOR (OR EQUIVALENT)	MATING CONTACT (OR EQUIVALENT)
J1 POWER	--	(4X) SIZE 16 PIN M39029/58-364	TV06RF-13-4S	SIZE 16 SOCKET M39029/56-352
J2 DEBUG/ STATUS	--	(37X) SIZE 22D PIN M39029/58-360	TV06RF-15-35S	SIZE 22D SOCKET M39029/56-348
J3 10GBASE-SR	--	(8X) SIZE 16 SOCKET TERMINUS M29504/05-4046	CF-504617-08P	SIZE 16 PIN TERMINUS M29504/04-4040
J4 10GBASE-T	--	(100X) SIZE 22D SOCKET M39029/56-348	TV06RF-23-35P	SIZE 22D PIN M39029/58-360
J5 10GBASE-T	--	(55X) SIZE 22D SOCKET M39029/56-348	TV06RF-17-35P	SIZE 22D PIN M39029/58-360

PINOUT – Digital Command Center The Tactician

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 13-4P KEYING “N”	A	IN	280VDC_IN
	B	OUT	28VDC_RTN
	C	---	SAFETY GROUND / CHASSIS
	D	---	NOT CONNECTED
	SHELL	---	CHASSIS

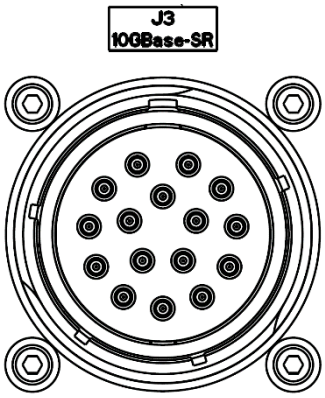


I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 (DEBUG/ STATUS) 15-35P KEYING “N”	1	OUT	CPU_RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	--	DEBUG_I2C_SCL
	5	--	DEBUG_I2C_SDA
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	MDIO_DATA
	10	--	MDIO_CLOCK
	11	--	GND
	12	BI	DEBUG_CPU_1GBASET_DA+
	13		DEBUG_CPU_1GBASET_DA-
	14		DEBUG_CPU_1GBASET_DB+
	15		DEBUG_CPU_1GBASET_DB-
	16		DEBUG_CPU_1GBASET_DC+
	17		DEBUG_CPU_1GBASET_DC-
	18		DEBUG_CPU_1GBASET_DD+
	19		DEBUG_CPU_1GBASET_DD-
	20	--	PIC_PROG_3.3V
	21	--	GND
	22	--	PIC_PROG_PGC
	23	--	PIC_PROG_MCLR
	24	--	PIC_PROG_PGD
	25	--	PIC_RS232_CONSOLE_TX
	26	--	PIC_RS232_CONSOLE_RX
	27	--	GND
	28-37	--	NOT CONNECTED
	SHELL	--	CHASSIS



PINOUT – Digital Command Center The Tactician

I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J3 10GBASE-SR 21-16S KEYING “N”	A	OUT	10GBASE-SR_TX	1
	B	IN	10GBASE-SR_RX	
	C	OUT	10GBASE-SR_TX	2
	D	IN	10GBASE-SR_RX	
	E	OUT	10GBASE-SR_TX	3
	F	IN	10GBASE-SR_RX	
	G	OUT	10GBASE-SR_TX	4
	H	IN	10GBASE-SR_RX	
	J	OUT	10GBASE-SR_TX	5
	K	IN	10GBASE-SR_RX	
	L	OUT	10GBASE-SR_TX	6
	M	IN	10GBASE-SR_RX	
	N	OUT	10GBASE-SR_TX	7
	P	IN	10GBASE-SR_RX	
	R	OUT	10GBASE-SR_TX	8
	S	IN	10GBASE-SR_RX	
	SHELL	---	CHASSIS	



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PINOUT - Digital Command Center The Tactician

I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J4 10GBASE-T 23-35S KEYING “N”	1	BI	10GBASE-T_DA+	9
	8		10GBASE-T_DA-	
	9		10GBASE-T_DB+	
	16		10GBASE-T_DB-	
	25		10GBASE-T_DC+	
	35		10GBASE-T_DC-	
	36		10GBASE-T_DD+	
	46		10GBASE-T_DD-	
	2	BI	10GBASE-T_DA+	10
	3		10GBASE-T_DA-	
	5		10GBASE-T_DB+	
	6		10GBASE-T_DB-	
	11		10GBASE-T_DC+	
	12		10GBASE-T_DC-	
	14		10GBASE-T_DD+	
	15		10GBASE-T_DD-	
	18	BI	10GBASE-T_DA+	11
	19		10GBASE-T_DA-	
	20		10GBASE-T_DB+	
	21		10GBASE-T_DB-	
	22		10GBASE-T_DC+	
	23		10GBASE-T_DC-	
	33		10GBASE-T_DD+	
	34		10GBASE-T_DD-	
	27	BI	10GBASE-T_DA+	12
	37		10GBASE-T_DA-	
	39		10GBASE-T_DB+	
	40		10GBASE-T_DB-	
	42		10GBASE-T_DC+	
	43		10GBASE-T_DC-	
	48		10GBASE-T_DD+	
	49		10GBASE-T_DD-	
	51	BI	10GBASE-T_DA+	13
	52		10GBASE-T_DA-	
	54		10GBASE-T_DB+	
	55		10GBASE-T_DB-	
	61		10GBASE-T_DC+	
	62		10GBASE-T_DC-	
	64		10GBASE-T_DD+	
	65		10GBASE-T_DD-	
	56	BI	10GBASE-T_DA+	14
	67		10GBASE-T_DA-	
	58		10GBASE-T_DB+	
	59		10GBASE-T_DB-	
	69		10GBASE-T_DC+	
	70		10GBASE-T_DC-	
	72		10GBASE-T_DD+	
	73		10GBASE-T_DD-	
	77	BI	10GBASE-T_DA+	15
	78		10GBASE-T_DA-	
	79		10GBASE-T_DB+	
	80		10GBASE-T_DB-	
	81		10GBASE-T_DC+	
	89		10GBASE-T_DC-	
	87		10GBASE-T_DD+	
	88		10GBASE-T_DD-	
	82	BI	10GBASE-T_DA+	16
	83		10GBASE-T_DA-	
	4		10GBASE-T_DB+	
	93		10GBASE-T_DB-	
	91		10GBASE-T_DC+	
	97		10GBASE-T_DC-	
	99		10GBASE-T_DD+	
	100		10GBASE-T_DD-	
	50, 74, 75, 98	--	SPARE	--
	Rest	--	GND	--

I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J5 10GBASE-T 23-35S KEYING “N”	1	BI	10GBASE-T_DA+	17
	8		10GBASE-T_DA-	
	9		10GBASE-T_DB+	
	16		10GBASE-T_DB-	
	25		10GBASE-T_DC+	
	35		10GBASE-T_DC-	
	36		10GBASE-T_DD+	
	46		10GBASE-T_DD-	
	2	BI	10GBASE-T_DA+	18
	3		10GBASE-T_DA-	
	5		10GBASE-T_DB+	
	6		10GBASE-T_DB-	
	11		10GBASE-T_DC+	
	12		10GBASE-T_DC-	
	14		10GBASE-T_DD+	
	15		10GBASE-T_DD-	
	18	BI	10GBASE-T_DA+	19
	19		10GBASE-T_DA-	
	20		10GBASE-T_DB+	
	21		10GBASE-T_DB-	
	22		10GBASE-T_DC+	
	23		10GBASE-T_DC-	
	33		10GBASE-T_DD+	
	34		10GBASE-T_DD-	
	27	BI	10GBASE-T_DA+	20
	37		10GBASE-T_DA-	
	39		10GBASE-T_DB+	
	40		10GBASE-T_DB-	
	42		10GBASE-T_DC+	
	43		10GBASE-T_DC-	
	48		10GBASE-T_DD+	
	49		10GBASE-T_DD-	
	51	BI	10GBASE-T_DA+	21
	52		10GBASE-T_DA-	
	54		10GBASE-T_DB+	
	55		10GBASE-T_DB-	
	61		10GBASE-T_DC+	
	62		10GBASE-T_DC-	
	64		10GBASE-T_DD+	
	65		10GBASE-T_DD-	
	56	BI	10GBASE-T_DA+	22
	67		10GBASE-T_DA-	
	58		10GBASE-T_DB+	
	59		10GBASE-T_DB-	
	69		10GBASE-T_DC+	
	70		10GBASE-T_DC-	
	72		10GBASE-T_DD+	
	73		10GBASE-T_DD-	
	77	BI	10GBASE-T_DA+	23
	78		10GBASE-T_DA-	
	79		10GBASE-T_DB+	
	80		10GBASE-T_DB-	
	81		10GBASE-T_DC+	
	89		10GBASE-T_DC-	
	87		10GBASE-T_DD+	
	88		10GBASE-T_DD-	
	82	BI	10GBASE-T_DA+	24
	83		10GBASE-T_DA-	
	4		10GBASE-T_DB+	
	93		10GBASE-T_DB-	
	91		10GBASE-T_DC+	
	97		10GBASE-T_DC-	
	99		10GBASE-T_DD+	
	100		10GBASE-T_DD-	
	50, 74, 75, 98	--	SPARE	--
	Rest	--	GND	--

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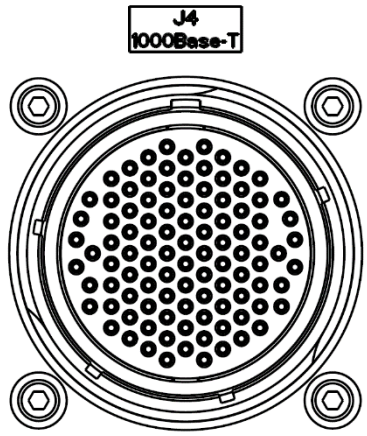
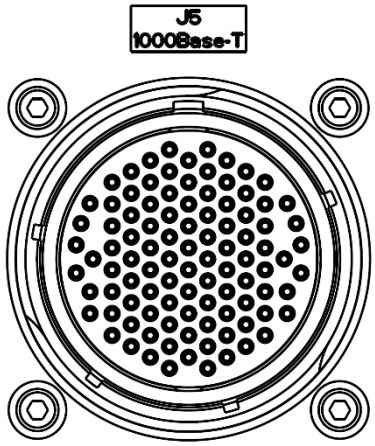
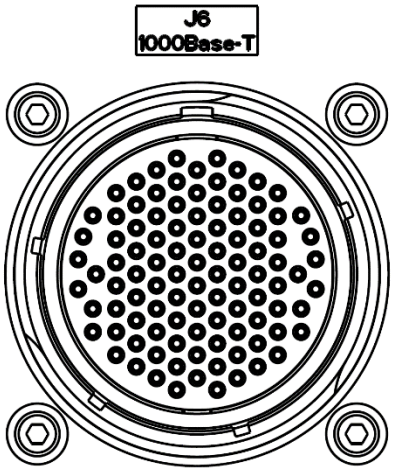
PINOUT - Digital Command Center The Tactician

I/O CHART				
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO.
J6 10GBASE-T 23-35S KEYING "N"	1	BI	10GBASE-T_DA+	9
	8		10GBASE-T_DA-	
	9		10GBASE-T_DB+	
	16		10GBASE-T_DB-	
	25		10GBASE-T_DC+	
	35		10GBASE-T_DC-	
	36		10GBASE-T_DD+	
	46		10GBASE-T_DD-	
	2	BI	10GBASE-T_DA+	10
	3		10GBASE-T_DA-	
	5		10GBASE-T_DB+	
	6		10GBASE-T_DB-	
	11		10GBASE-T_DC+	
	12		10GBASE-T_DC-	
	14		10GBASE-T_DD+	
	15		10GBASE-T_DD-	
	18	BI	10GBASE-T_DA+	11
	19		10GBASE-T_DA-	
	20		10GBASE-T_DB+	
	21		10GBASE-T_DB-	
	22		10GBASE-T_DC+	
	23		10GBASE-T_DC-	
	33		10GBASE-T_DD+	
	34		10GBASE-T_DD-	
	27	BI	10GBASE-T_DA+	12
	37		10GBASE-T_DA-	
	39		10GBASE-T_DB+	
	40		10GBASE-T_DB-	
	42		10GBASE-T_DC+	
	43		10GBASE-T_DC-	
	48		10GBASE-T_DD+	
	49		10GBASE-T_DD-	
	51	BI	10GBASE-T_DA+	13
	52		10GBASE-T_DA-	
	54		10GBASE-T_DB+	
	55		10GBASE-T_DB-	
	61		10GBASE-T_DC+	
	62		10GBASE-T_DC-	
	64		10GBASE-T_DD+	
	65		10GBASE-T_DD-	
	56	BI	10GBASE-T_DA+	14
	67		10GBASE-T_DA-	
	58		10GBASE-T_DB+	
	59		10GBASE-T_DB-	
	69		10GBASE-T_DC+	
	70		10GBASE-T_DC-	
	72		10GBASE-T_DD+	
	73		10GBASE-T_DD-	
	77	BI	10GBASE-T_DA+	15
	78		10GBASE-T_DA-	
	79		10GBASE-T_DB+	
	80		10GBASE-T_DB-	
	81		10GBASE-T_DC+	
	89		10GBASE-T_DC-	
	87		10GBASE-T_DD+	
	88		10GBASE-T_DD-	
	82	BI	10GBASE-T_DA+	16
	83		10GBASE-T_DA-	
	4		10GBASE-T_DB+	
	93		10GBASE-T_DB-	
	91		10GBASE-T_DC+	
	97		10GBASE-T_DC-	
	99		10GBASE-T_DD+	
	100		10GBASE-T_DD-	
	50, 74, 75, 98	--	SPARE	--
	Rest	--	GND	--







Amphenol Ruggedization Design

OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

TEMPERATURE:

- Operating Temperature- Thermal Cycles between -40°C and 85°C while device is operating
- Temperature is measured at chassis housing or card edge
- Storage Temperature- Thermal Cycles between -55°C and 125°C

HUMIDITY:

- Operating Humidity- Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity- Humidity cycle between 0-100% condensing humidity

SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION:

- Sine Vibration - 10g Peak, 5-2,000Hz
  - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
  - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
  - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

FLUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTRONMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
- Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL- HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

Amphenol
MILITARY HIGH SPEED

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