Amphenol
MILITARY HIGH SPEED

M4094 SERIES

DC/DC POWER SUPPLY



PRODUCT HIGHLIGHTS

- VITA 62.2 COMPLIANT
- SOSA™ ALIGNED
- 3U FORM FACTOR
- UP TO 800 W
- OPERATING TEMP: –55°C to +85°C
- EMI: Compliant to MIL-STD-461G
- Environmental: MIL-STD-810
- Input Options:
  - MIL-STD-704
- Cyber secure

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MILITARY HIGH SPEED

M4094 VPX DC/DC POWER SUPPLY

SPECIAL FEATURES

- VITA 62.2 Compliant
- Aligned with the SOSA™ Technical Standard
- Wide input range
- Connectors are VITA 62.2 to increase breakdown voltage
- Up to 800W output power
- Remote sense
- Fixed switching frequency (250 kHz)
- External synchronization capability
- Indefinite short circuit Protection
- Over-voltage shutdown with auto-recovery
- Reverse battery protection
- Over temperature shutdown with auto-recovery
- EMI filters included
- System Management: protocol per VITA 46.11
    - Output voltages and currents
    - Input voltage
    - Card temperature
    - Card system status

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Electrical Specifications

DC Input
$270V_{DC}$

- Works Through MIL-STD-704 (A-F) Normal and Abnormal Steady State
- Works Through MIL-STD-704(E-F) Normal transients
- Protected MIL-STD-704(B-D) Normal/Abnormal Transients
- Protected MIL-STD-704(E-F) Abnormal Transients

DC Output

VS1:	12V	up to 64A
3.3VAux:	3.3V	up to 15A

Isolation
Over 20 MΩ at test voltage:
500V between Input to Output and case (while Output & Case shorted together).
100V between Output to Case.

Efficiency
Up to 91%

EMC
Designed to meet:
MIL-STD-461G CE101, CE102, CS101, CS114, CS115, CS116

Line/Load regulation
See table 2

Ripple and Noise
Typically, less than $50mV_{p-p}$ (max. $1\%_p$). Measured across a 0.1µF capacitor and 10µF capacitor on load across Temperature Range.

System management options:

1) I2C
2) IPMI
3) VITA 46.11 Tier II IPMC

Data available:

- Output voltages and currents
- Input voltage
- Card temperature
- Card status

Load Transient Overshoot and Undershoot
Output dynamic response of less than 5% at load Step of 60%-90%.
Output returns to regulation in less than 1mSec

Normal Quiescent Current:
Inhibited Output: 20mA (3.3VAux Only)
Disabled Input: 17mA (All Outputs Off)

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Environmental [1]

Design to Meet MIL-STD-810G

Temperature

Operating: –55°C to +85°C at unit edge
Storage: –55°C to +125°C

Designed to meet 600 thermal cycles durability test

Altitude

Method 500.5, Procedure I & II Storage/Air Transport: 40 kft
Operation/Air carriage: 70 kft

Salt Fog:

Method 509.5

Fungus

Does not support fungus growth, in accordance with the guidelines of MIL- STD-454, Requirement 4.

Humidity

Method 507.5, Up to 95% RH

Shock

Method 516.6
40g, 11msec saw-tooth (all directions)

Vibration

Vibration: Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)

Reliability: 375,135 Hours, calculated IAW MIL-HDBK-217F Notice 2 at +65 °C, GF

Note 1: ***Environmental Stress Screening (ESS)*** Including random vibration and thermal cycles is also available. **Please consult factory for details.**

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Protections [1]

Input

- **Inrush Current Limiter**
  Peak value of 5 x I_{IN} for initial inrush currents lasting more than 50µSec.
- **Under Voltage**
  Unit shuts down when input steady state voltage drops below 200V_{DC}.
  Automatic restart when input voltage returns to nominal range.

Output

- **Passive over voltage protection on Aux outputs**
  Transorb, selected at 25% ± 5% above nominal voltage, is placed across the output for passive voltage limit.
- **Active over voltage protection on VS# outputs**
  20% ± 5% above nominal voltage.
  Automatic recovery when output voltage drops below threshold.
- **Overload / Short-Circuit protection**
  Continuous protection (10-30% above maximum current) for unlimited time (Hiccup).
  Automatic recovery when overload/short circuit removed.

General

- **Over Temperature Protection**
  Automatic shutdown at internal temperature of 95 ± 5°C.
  Automatic recovery when temperature drops below 90 ± 5°C.

Note 1: Thresholds and protections can be modified / removed (please consult factory)

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Functions and Signals - According to VITA 62

Signal Name	Type	Description
FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2 [1]
SYSRESET*	Output	Indicates to other modules in the system that all outputs are within their working level. Please refer to Figure 2 [1]
INHIBIT*	Input	Controls power supply outputs. This signal in conjunction with **ENABLE** controls the outputs. Please refer to Table 1 and Figure 1 [1]
ENABLE*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1 [1]
GA0*, GA1*, GA2*	Input	Used for geographical addressing. GA2 is the most significant bit and GA0 is the least significant bit. [1]
SCL_A, SDA_A	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. [1]
SCL_B, SDA_B	Bidirectional	Redundant I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. [1]
Sync_In	Input	The Sync_In signal is used to allow the power supply frequency to sync with the system frequency. [1] Optional.
VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
3.3Vaux A.C.S	Bidirectional	Support 3.3Vaux Active current share between Outputs. See Current Share para. [1] [2] [3] (Optional, non-SOSA configuration)
PO#_*SHARE*	Bidirectional	Support current share between Outputs[1]
Alert Bit	Output	Indicates to other modules in the system about Input Voltage loss. Please refer to Figure 2 [1] [2]

Notes:
1. Signal referenced to **SIGNAL RTN**.
2. When not used leave open
3. For 3.3Vaux in passive or Non-Current Share configuration, this pin is Internally Disconnected

Table 1 – Inhibit and Enable Functionality

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
VS1	OFF	OFF	ON	OFF
3.3V	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage

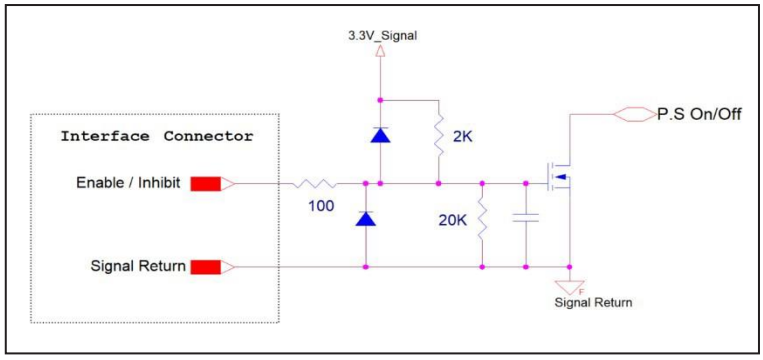


Figure 2 – SysRst and Fail bit Output Stage

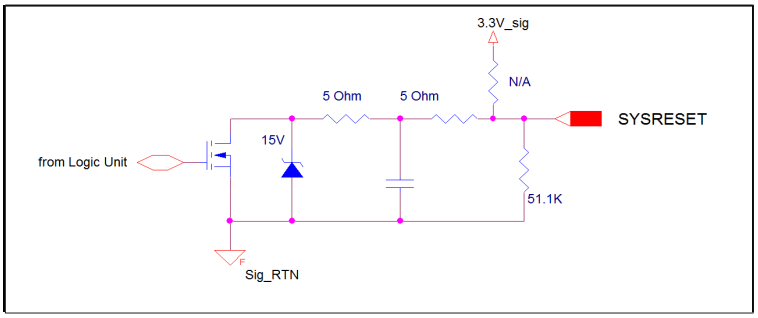
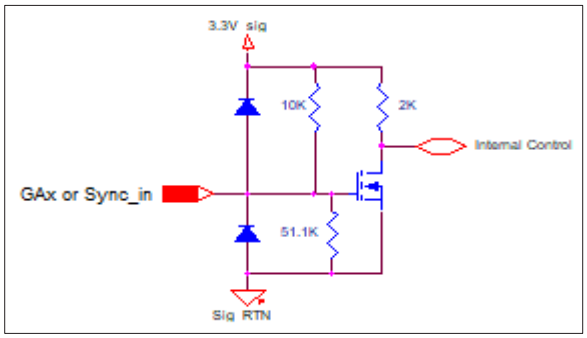
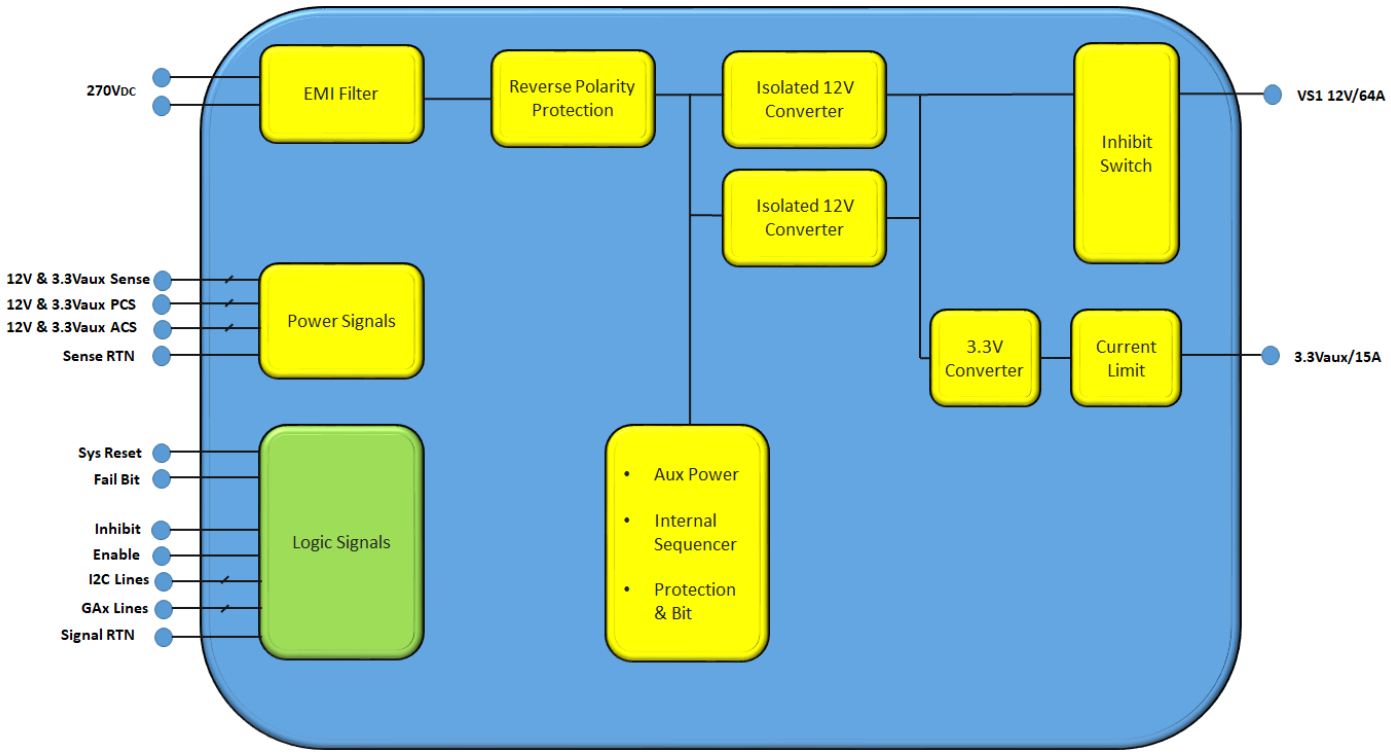


Figure 3 – GAx and Sync_In Stage



Simplified Block Diagram



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Detailed Information

1. M4094 Input Voltage Operation.

The M4094 steady state operation is per Mil-STD-704. Unit will work thorough all Mil-STD-704E/F Transients. Unit is protected during Abnormal transients and interrupts.

2. Outputs Voltage Regulation

The M4094 contains accurate internal sense lines to keep output voltage at less than 2% regulation for all Line/ Load and temperature range (see Table 2).

Output Voltage Range	12V/64A	3.3V/15A
Active Current Share	11.85V - 12.15V	3.28V - 3.42V
Passive Current Share	N/A	3.25V - 3.45V

Table 2: Outputs voltage regulation. Temperature -55 to 85 °C

2.1. Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop. *Sense Lines* proper connection is shown in Figure 3.

Each VSx output has its own *Sense Lines*, additional common *Sense RTN Line* is provided for all VSx Outputs (VITA 62 Standard).

Contact Factory for Sense configuration different than the VITA 62 standard

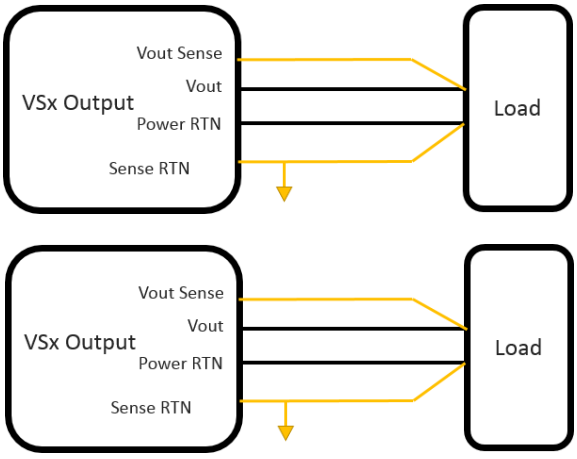
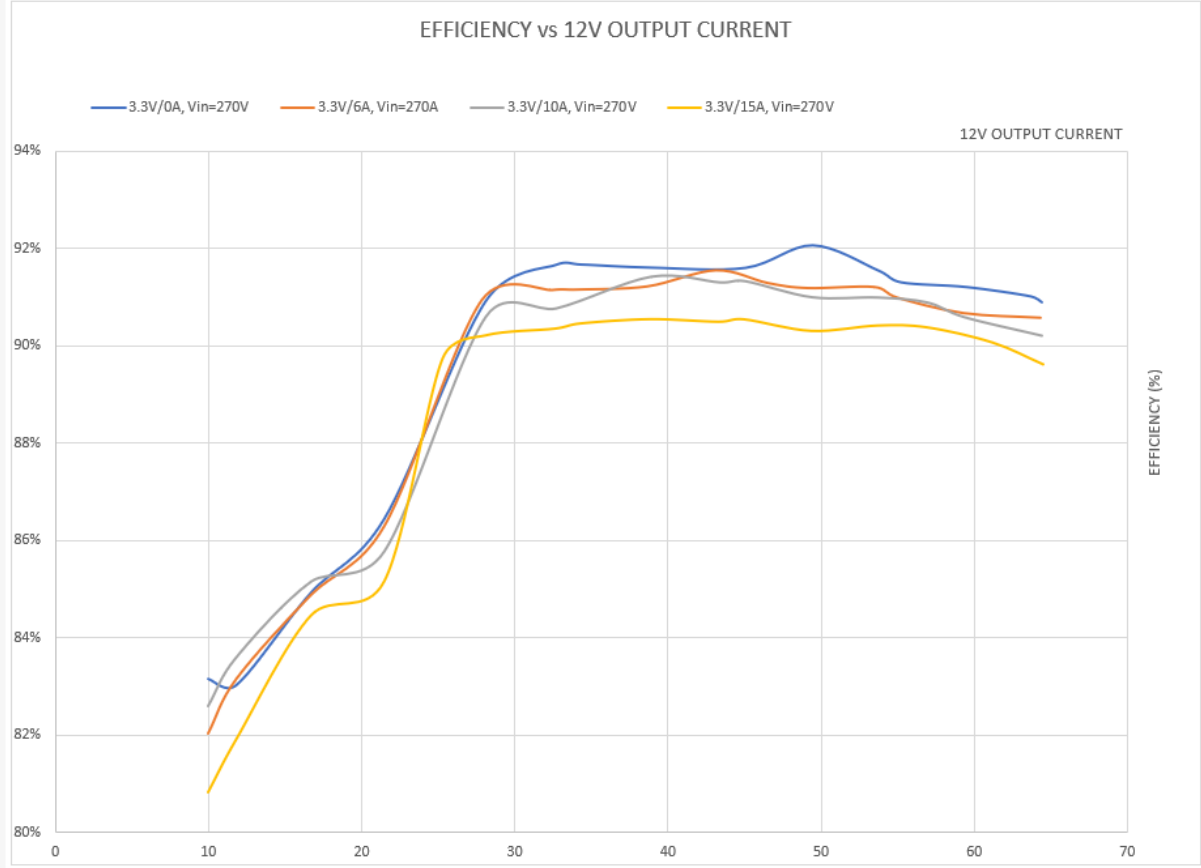


Figure 4: M4094 Sense line connection

2.3. Efficiency

Efficiency curve at 270V line room temperature



3. Current Share (C.S)

Current Share of two or more units is optional (Contact Factory)
Unit can support parallel configuration of two units. VS1 & VS2 and Aux will current share with about 5-10% load balance.
The unit can support two methods of current sharing:

3.1 Passive Current Sharing (P.C.S)

Current sharing is done in open loop, output voltage drops as a function of output load.
Load Balance of about 5-10% load is expected.

3.2 Active current sharing (A.C.S)

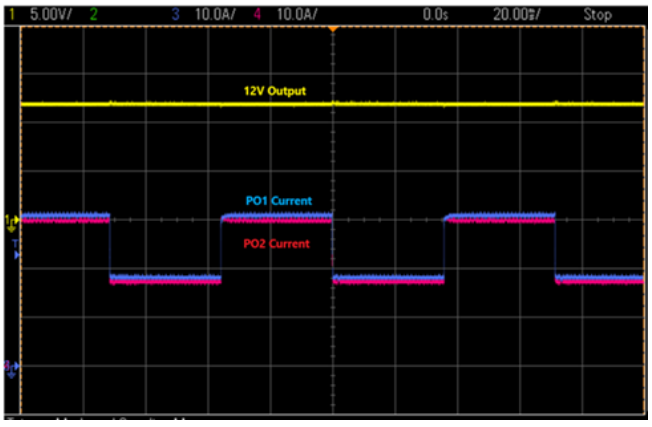
Current sharing is done in a closed loop. All paralleled outputs are compared and feedback is used to balance their load current. The result is a more stable, less sensitive output voltage without voltage drop.
Load Balance of about 2-5% load is expected.

3.3 Current share connection between two Units.

For a required output to current share please connect the following Pins between the two units

- *PO#_Sense* & *PO#_Sense_RTN* (for best performance, Pins from paralleled units should be connected to a single point and as close as possible to the load point)
- *VS1_SHARE (A7)*
- *VS1_ ACS (C7)*
- *3.3Vaux_SHARE (B7)*
- *3.3Vaux_ACS (D1)* Optional[1] [2]

Typical ACS Dynamic Load of Two 12V Paralleled Outputs



Notes

1. When not used, 3.3Vaux A.C.S can be left open.

   When ordering 3.3Vaux P.C.S or 3.3Vaux Non-Current Share unit, this pin is Internally disconnected

2. 3.3Vaux ACS (Pin D1) is not required by SOSA and is optional.

4 Communication Protocol

Unit communication protocol can be configured as VITA 46.11 Tier 2 IPMC or Custom IPMI compatible protocol. For more details on IPMI or VITA 46.11 protocol refer to para. 4.1 or 4.2 respectively below.

4.1 Custom IPMI Protocol

Electrical Parameters

Vcc: 3.3VDC
Pull-up: 2.2kOhm
Input capacitance: 100pf

Slave Device Addressing

- 256 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Protocol
- Support Slot Addressing per VITA 62

	MSB							LSB
Slot Number	A6	A5	A4	A3	A2/GA2*	A1/GA1*	A0/GA0*	R/W
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	

* Slot location is determined by GAx per VITA 62.

Communications Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request)
The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

S	Slave Address	R/W	A	DATA	A	DATA	A	DATA	A	• • •	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes
S -Start
P- Stop

Master Transmit	Unit Transmit

Memory Space

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		21 Hex
1		N/A		00 Hex
2-3	S Integer, MSB First	Temperature -55C to 120C	T(C°)=+/- 7bit Dec	-55°C to 125°C
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data· m2	20.48V
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data· m2	20.48V
8-9	U Integer, MSB First	N/A	N/A	N/A
10-11	U Integer, MSB First	N/A	N/A	N/A
12-13	U Integer, MSB First	N/A	N/A	N/A
14-15	U Integer, MSB First	N/A	N/A	N/A
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data· m3	80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data· m3	20A
20-21	U Integer, MSB First	N/A	N/A	N/A
22-23	U Integer, MSB First	N/A	N/A	N/A
24-35	U Integer, MSB First	N/A	N/A	N/A
26-27	U Integer, MSB First	N/A	N/A	N/A
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	M4094-xxx* (Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec (Note2)	Optional
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	Optional
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	Optional
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	4 digits
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256	

Note:

M2 = 20.48/65535

M3 = 80/65535

M4 = 20/65535

* Matching unit part number

Notes 1 to 5

1. Part Number Example: M4465

Byte No'	32	33	34	35	36	37	38	39-51
Character	M	4	4	6	5	(-)	4	0
Hex	4D	34	34	36	35	2D	34	00

2. Serial Number Example: 25

Byte No'	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

3. Date Code Example: week 35 of 2018

Byte No'	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

4. Hardware Rev Example: B01 Rev (-), B01 Rev A

Byte No'	58	59
Character	(-)	A
Hex	2D	41

5. Firmware Rev Example: 2.1.0.0

Byte No'	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

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4.2 VITA 46.11 Tier 1 IPMC Protocol

Please see *46.11 User Manual* for detailed information of operation.

Sensors included are seen in the table below.

Units are designed to be upgradable to 46.11 Tier 3 compliance upon release of that specification

Record ID	Sensor ID	Sensor Type	Name
0000	00	F0h	FRU State Sensor
0001	01	F1h	System IPMB Link Sensor
0002	02	F2h	FRU Health Sensor
0003	03	02h	FRU Voltage Sensor
0004	04	F3h	FRU Temperature Sensor
0005	05	F4h	Payload Test Results Sensor
0006	06	F5h	Payload Test Status Sensor
0100	07	02h	VS1 Voltage
0103	0A	02h	3.3Vaux Voltage
0106	0D	03h	VS1 Current
0109	10	03h	3.3Vaux Current
010C	13	01h	Analog Temperature
9999	N/A	N/A	Device Management

5. Sync In and Switching Frequency

Standard switching frequency with no Sync In signal applied is 220kHz ±5%.

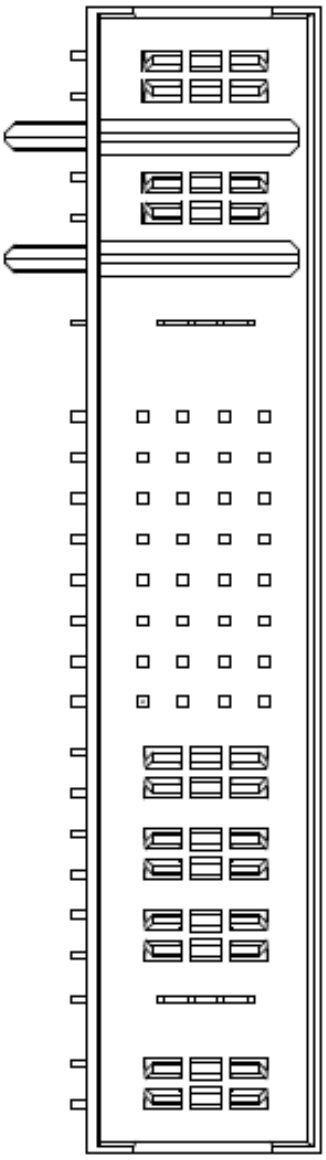
When optionally configured to have Sync In functionality the unit will sync to a signal between 200kHz and 300kHz ±5%. The square wave must be at 3.3V CMOS standard logic levels with a duty cycle between 20% and 80%.

The M4094 will sync after 32 cycles of within tolerance external clock cycles. The unit will revert to its internal clock frequency upon any out of specification clock cycles and will need 32 good cycles to resync to the external clock.

Contact factory to add Sync_in functionality and to customize its configuration values.

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ROWS	POWER	SIGNAL									POWER				
	P1	P2	LP1	1	2	3	4	5	6	7	8	P3	P4	P5	LP2	P6
D				Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5					
C				Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5					
B	TT	TT	LT	R5	R5	R5	R5	R5	R5	R5	R5	TT	TT	TT	LT	TT
A				D5	D5	D5	D5	D5	D5	D5	D1					

2ACP+1LP+32S+3HDP+1LP+1HDP

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Pin Assignment

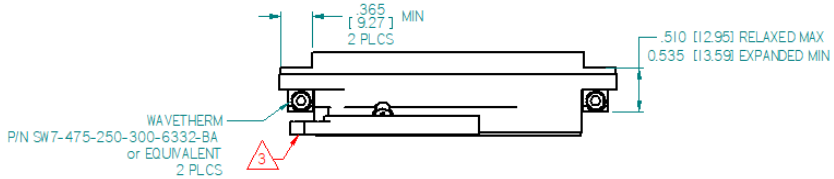
Pin Number	*Pin Name*
P1	-DC_IN
P2	+DC_IN
LP1	CHASSIS
P3	VS1
P4	POWER_RETURN
P5	POWER_RETURN
LP2	3.3Vaux
P6	VS1
A8	VS1_SENSE
B8	3.3Vaux _SENSE
C8	VS1_SENSE / N.C
D8	SENSE_RETURN
A7	VS1_SHARE
B7	3.3Vaux _ SHARE
C7	VS1_ACS
D7	SiG_RTN
A6	SCL_B
B6	SDA_B
C6	N.C.
D6	SYSRESET*
A5	GA0*
B5	GA1*
C5	SCL_A
D5	SDA_A
A4	N.C.
B4	N.C
C4	N.C
D4	N.C
A3	Sync_In / N.C.
B3	N.C.
C3	N.C (NED)
D3	N.C (NED RETURN)
A2	N.C.
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	N.C.
B1	N.C.
C1	GA2*
D1	3.3Vaux_ACS / N.C.

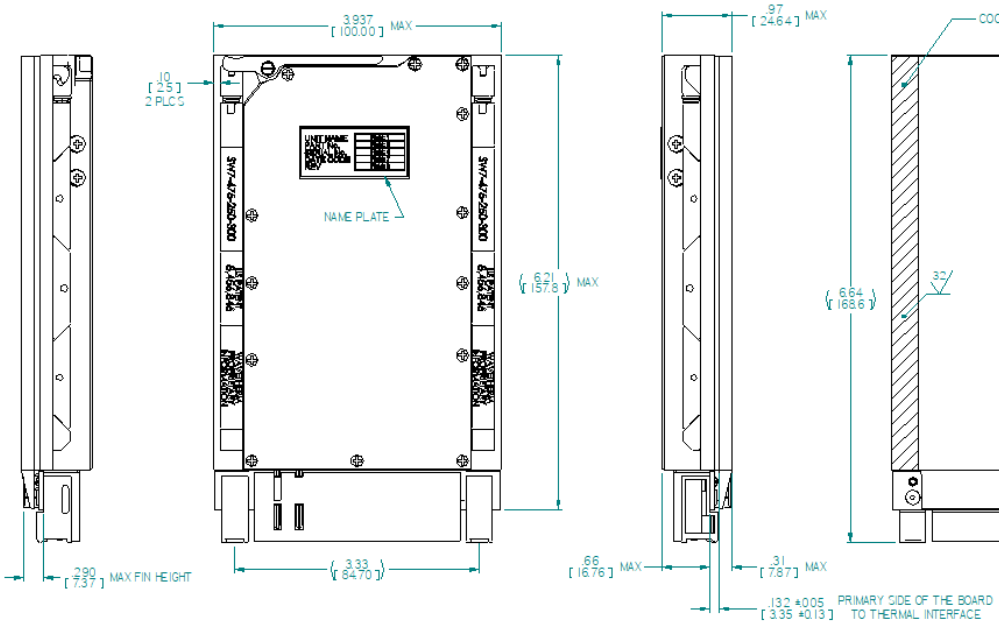
Notes:
Pin assigned as Function/N.C is optional and can be configured as not connected
Previous configurations had 3.3Vaux_ACS on Pin B4 and Sync_In (labeled as Ref Clk(+)) on Pin A1.
Pin D1 was previously labeled as Alert/N.C. and was unused.
Pin A3 was previously labeled as Ref_Clk (-) / N.C. and was unused

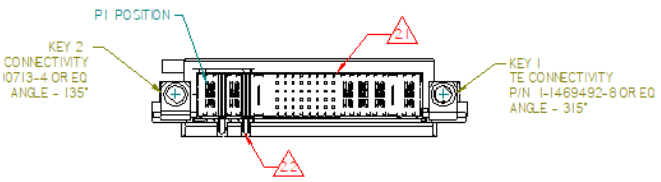
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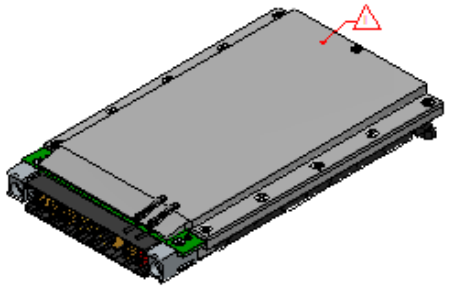
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Outline Drawing



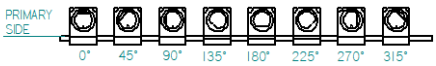






COVERS:
LUMINUM ALLOY 6061-T651 & 5052-H32)
MICAL CONVERSION COATING MIL-DTL-5541,TYPE 1, CLASS 1A
D BARRIER:
R TE CONNECTIVITY P/N 2313442-1 OR EQ.
4 TE CONNECTIVITY P/N 2313441-1 OR EQ.
SERT, P/N 2313445-1.
CTOR
LUMINUM ALLOY 6061-T651)
CK ANODIZE PER MIL-A-8625,TYPE II,CLASS 2
SHALL BE MIL-STD-454, REQT. 9

KEYING ORIENTATION GUIDE PER ANSI VITA 46.0



VITA 62 3U PRIMARY SIDE RETAINERS COMPATIBLE

DIMENSIONS ARE IN [IN]
DO NOT SCALE DRAWING

GENERAL TOLERANCES
.XX ± .02
.XXX ± .010
ANGELES ± .5°

*** Specifications a** Weight: Approx. 800 g (24.34)

notice by the manufacturer.

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