M7049-103 Datasheet

28Vdc output, 750W Switching-regulator Module for Permanent Magnet Generator (PMG) applications.

(The M7049-103 is identical to the M7049-102 but without the "Piggyback I/O Filter board.)



Main Features

- **900W/30 sec. Over-load capability**
- **Up to 8 Modules can be paralleled (current-share), supporting up to 6KW load (7.2KW for 30 seconds).**
- **Built-in EMI Input & Output Filters**
- **30 to 200 VDC input voltage range, compatible with the rectified output of most PMG's.**
- **Crowbar over voltage protection**
- **Overload, Over-voltage, and Over-temp protections**
- **No external capacitors required**
- **No minimum load required**
- **Base-plate cooled (by external heatsink)**
- **On/Off input and BIT output.**
- **Remote Sense lines.**
- **Upon request, the output voltage can be factory trimmed above or below 28Vdc.**

General Description

M7049-103 is a 750W high efficiency switching regulator, that when fed from the rectified output of a 3-phase Permanent Magnet Generator (PMG), will provides a well-regulated, filtered, and protected 28VDC Output. The M7049-103 is designed for parallel current-sharing operation, allowing the user to parallel up to eight M7049-103 units and supports up to 6KW (7.2KW for 30 sec.). For typical application see Figure 1.

Note: P/N M7049-103 is identical to M7049-102 but without the pre-assembled "Piggyback" I/O filter board that provides additional filtering and convenient Bus-bars terminals. The M7049-103 is intended for users who cannot accommodate the additional 16mm that the I/O filter board adds to the 42mm depth of the Module.

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com

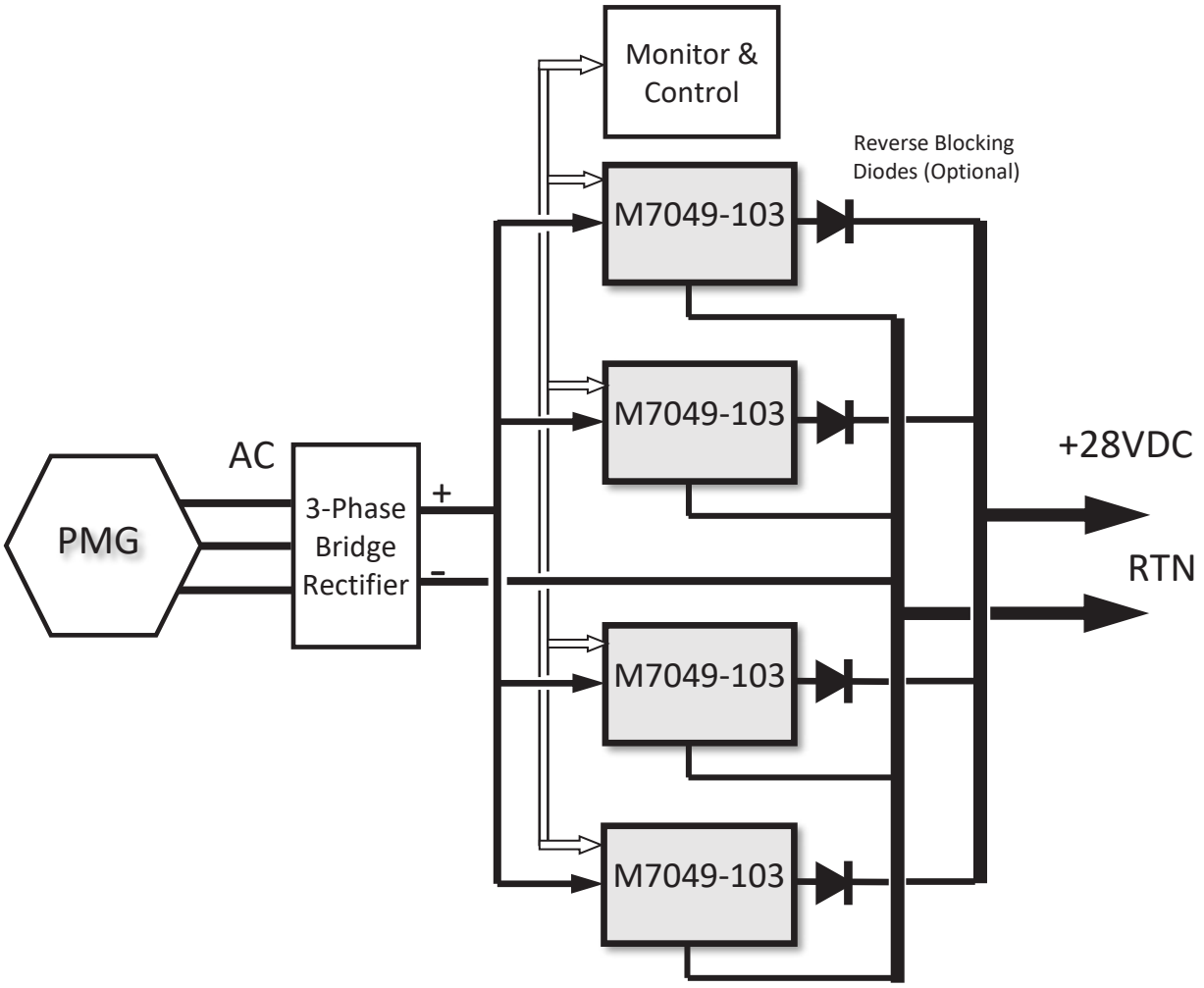


Figure 1: M7049-103 Typical Application, 28VDC/3KW Supply

How to Order:

Part Number
M7049103

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com

Absolute Maximum Ratings

Exceeding the limits below may damage the unit.

PARAMETER	LIMITS
Input Voltage	+230Vdc / -0.5VDC
Input Voltage Max. Rate of Change	15 V/mS
Output Voltage (externally applied)	+33Vdc / -0.5Vdc
ENABLE to ENABLE_RTN	+12Vdc /-30Vdc (higher voltage may be applied if the current is limited to 15mA)
BIT Voltage	+39Vdc /-0.5Vdc
BIT Current	5mA
All Pins to Chassis	500V
Power Terminals to ENABLE and BIT pins	200V
ENABLE pins to BIT pins	200V

Environmental

The M7049-103 will operate without degradation when subjected to the environment below.

Exceeding these limits may damage the unit.

PARAMETER	LIMITS
Shock	30g/11mS, Terminal Peak Sawtooth per MIL-STD-810G, Fig 516.6-10
Vibration	Per MIL-STD-810G, Figure 514.6E-1, but aggravated from $0.04g^2/Hz$ to $0.05g^2/Hz$.
Acceleration	10 G, all directions per MIL-STD810G, Method 513.6, Procedure II
Operating Temperature	Ambient: -40°C to +71°C The temperature of the Cooling base should be maintained below +90°C
Storage Temperature	-55°C to +80°C (Ambien temperature)
Humidity	100% RH per MIL-STD-810G, Method 507.5, Procedure II (Aggravated)

Size and Weight

The M7049-103 is 92mm (3.62") wide, 93.7mm (3.69") high, 42mm (1.65") deep (exc. the I/O pins) and weighs 500gr. For detailed outline dimensions and mounting provisions, see DWG M7049003.

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com

ELECTRICAL CHARACTERISTIC

Unless otherwise specified: Vin = 30 to 200 Vdc, T(amb) = -40°C to +71°C, T(base) ≤ 85°C.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.
Turn-on Input Voltage	No load to 750 W	**24Vdc**	**27Vdc**	**30Vdc**
Turn-on Time (1)	From ENABLE Input changes from L to H to Vout>27VDC. No load to 750 W	**10mS**	**30mS**	**50mS**
Turn-on Overshoot(1)				**29VDC**
Output Power	Continuous	**750 W**		
	30 seconds Overload (Vin>70 Vdc)	**900 W**		
Output Voltage	No load to 750 W	**27.5 Vdc**	**28.0Vdc**	**28.5 Vdc**
	900W (Overload), (Vin>70 Vdc)	**26.5 Vdc**		**28.5 Vdc**
Current Limit		**32A**	**35A**	**38 A**
Current-share error (2)	All modules have identical harness, all LS pins are tied together, all			**±3A**
Efficiency (3)	Vin = 100 Vdc @ 750W	**92.5%**	**93.5%**	
No-load Consumption				**2W**
Isolation	All signals to chassis, at 500VDC	**10MΩ**		
	Common to BIT & ENABLE, ENABLE to BIT @ 200VDC	**10MΩ**		
Output ripple (4)	10 Hz to 20 MHz, No-load to 750W		**0.1Vrms**	**0.3 Vrms**
Output Over Voltage Protection Threshold	Electronic (5)	**31.5 Vdc**		**32.5 Vdc**
	Crow-bar (5)	**34.5 Vdc**		**36.5 Vdc**
ENABLE Logic Levels (6)	Output Disabled			**1.0 V**
	Output Enabled	**3.5 V**		
BIT Output (6)	Vout < 24.5 Vdc, or internal failure detected.	**Open, I<0.1mA @33Vdc**		
	Vout > 26.5 Vdc, no internal failure detected.	**Active Low, V<0.5V @ 2mA**		
Over Temperature Protection Thresholds	Shutdown (Base plate temperature)	**92°C**	**95°C**	**98°C**
	Auto recovery	**10±2° below Shutdown Temp.**		
Temperature Monitor	Base-plate mounted Thermistor, Vishay 2381-640-63103			

Notes:

1. See Figures 7 and 8.
2. The Current Share Error (CSE) is equal to: $I_{(Module)} - (I_{(load)}/N)$ when N is the number of paralleled modules that drive the load current $I_{(Load)}$.
3. See Figures 4 and 5.
4. Measured on resistive load with capacitance of 1µF or higher.
5. See Overvoltage Protection in the Application section Deleted.
6. See Figure 3.

PINOUT

J1- Signal Connector (Harwin P/N M80-5401042 or eq.)

Pin #	Des.	I/O	Function
1	-SNS	I	Negative remote sense line
2	LS	I/O	Load Share
3	N/A	-	Not used
4	BIT	O	BIT output
5	BIT_RTN	I	The return line of the BIT signal
6	+SNS	I	Positive remote sense line
7	TEMP-1	O	One terminal of the Temp Sensing thermistor
8	TEMP-2	O	Second terminal of the Temp Sensing thermistor
9	ENABLE	I	Enables the 28VDC output
10	ENABLE_RTN	I	The return line of the Enable signal

Power Terminals (2mm Gold-plated pins, see Figure 2)

Pin #	Des.	I/O	Function
P1	+DC_IN	I	Positive DC Input
P2	COMMON	I/O	Common return of both Input and Output
P3	+28VDC	O	+28VDC Output

See DWG M7094003 for the exact location of J1 and the Power Pins.

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
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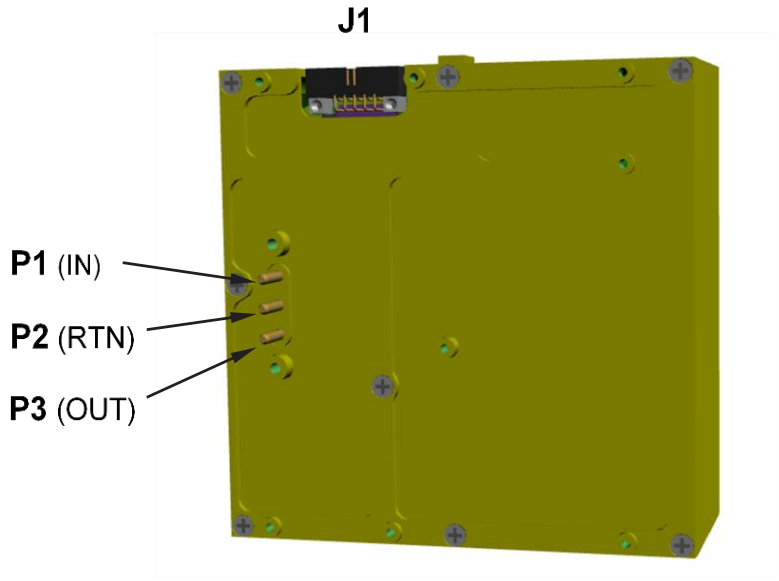


Figure 2: M7049-103 Power Terminals

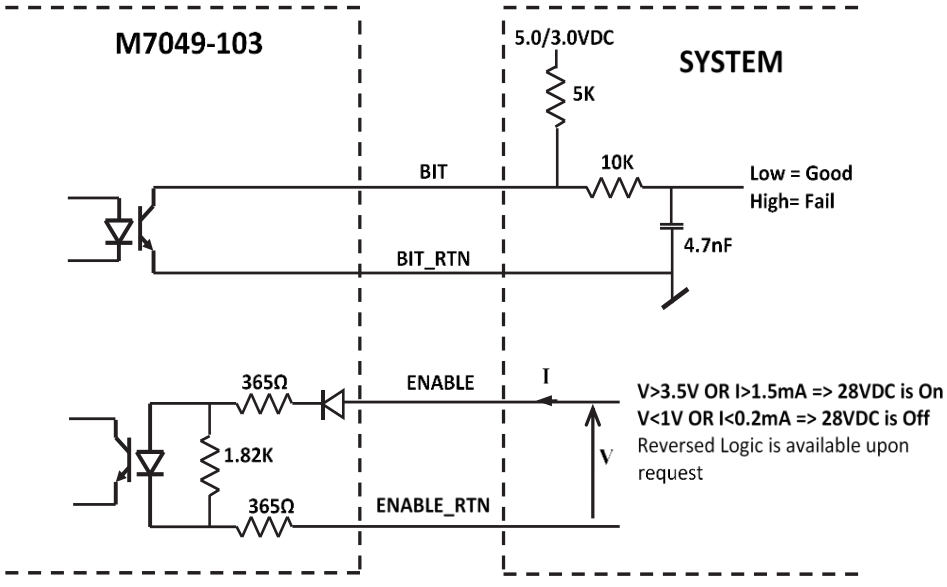


Figure 3: M7049-103 Logic Signals Interface

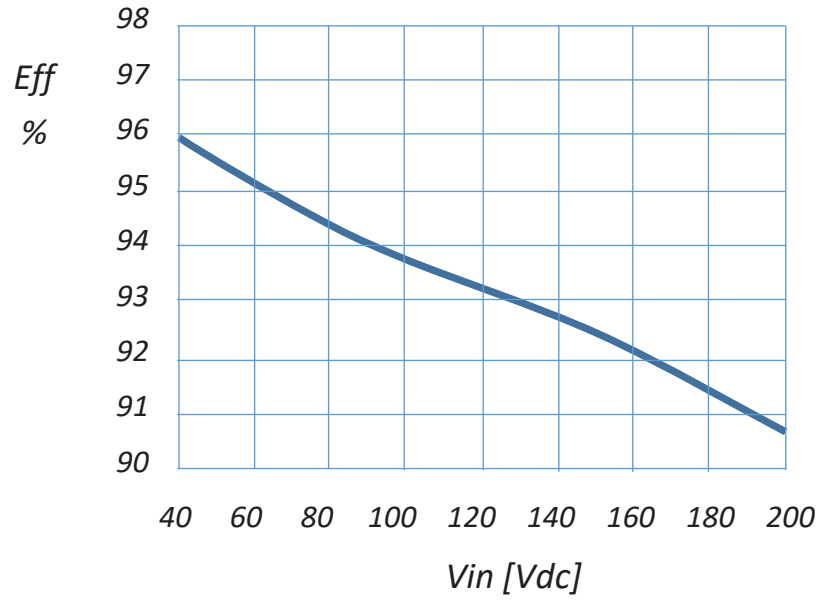


Figure 4: Typical Efficiency at 750W Vs. Input Voltage

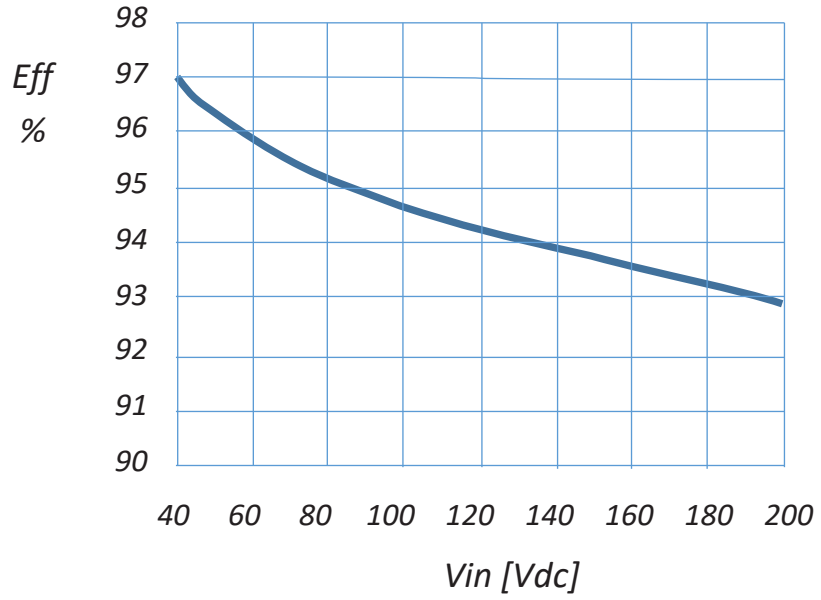


Figure 5: Typical Efficiency at 375W Vs. Input Voltage

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
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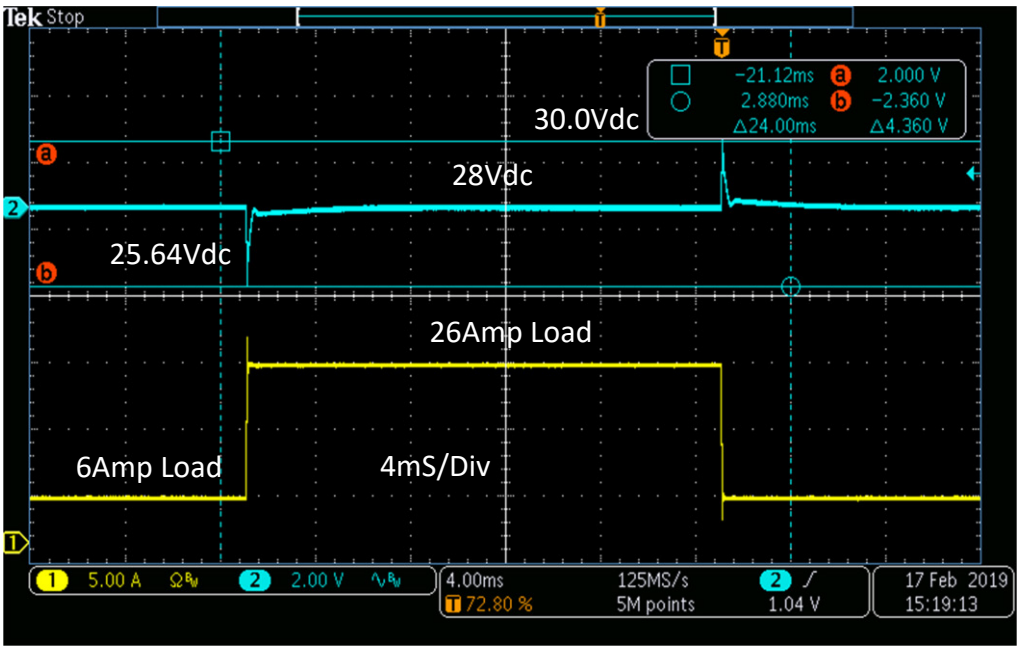


Figure 6: Typical Step-load Response, 6 to 26 Amp

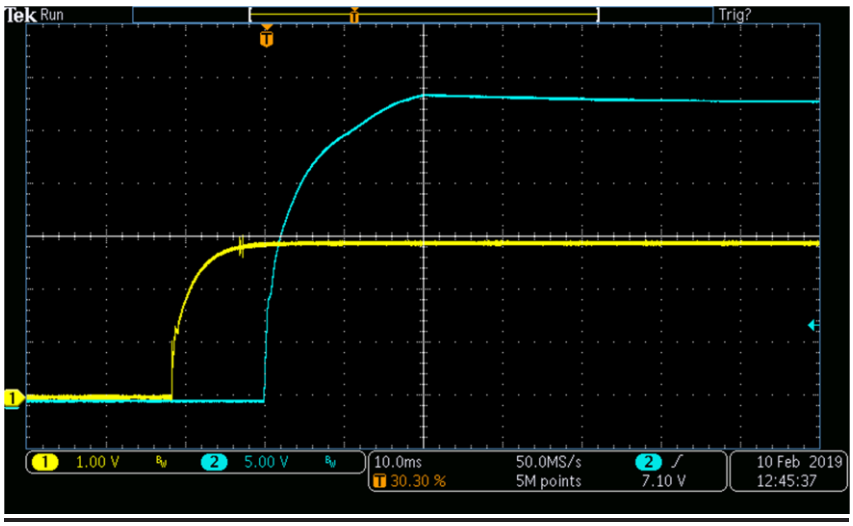


Figure 7: Typical Turn-on at No-load and 100VDC Input

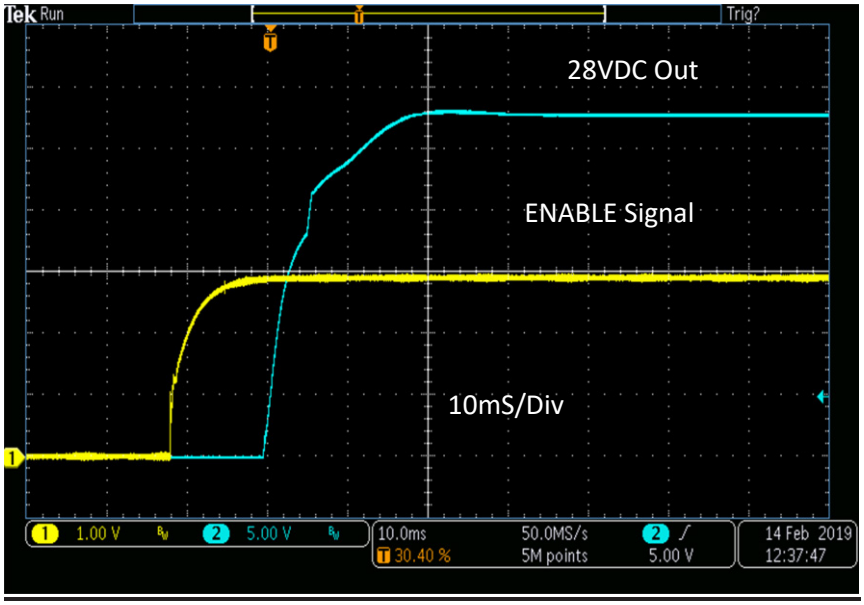


Figure 8: Typical Turn-on at 26Amp Load and 100VDC Input

APPLICATION INFORMATION

Input Source and Grounding

The M7049-103 is a "3-port" switching regulator, its input (T1) and 28VDC output (T3) are isolated from chassis, but not from each other and share a Common RTN (T3) terminal. **It means that the AC output of the PMG must remain floating and except for the 3-phase rectifier that powers the M7049-103 module(s) should remain isolated and should not be used by any load that may provide a current path to chassis. Typically, the 3-phase rectifier that feeds the M7049-103 module(s) should be the only load on the PMG AC output**.

Testing the M7049-103 in a Laboratory Setup.

In a typical application the M7049-103 is permanently connected to the power source (a 3-phase rectifier fed by a PMG) and as the RPM of the PMG rises, the input voltage to the M7049-103 rises too and gradually charges the input capacitors of the Module with negligible inrush-current. When testing the M7049-103 in a laboratory setup, using a laboratory DC or AC source (instead of a PMG) care should be taken not to apply the input voltage to the M7049-103 in an abrupt manner. When using a typical laboratory power supply, activating the Power On switch will result in a moderate rise time that is much slower than the 15V/mS limit of the M7049-103 (and therefore will not cause any issue). Care should be taken not to use a switch (or a relay) between the laboratory power supply output to the M7049-103 input, and if such a switch is unavoidable, to make sure that the switch is On before the laboratory power supply is turned on.

Parallel Connection

When several M7049 Modules are used in parallel (Figure 1), the following considerations should apply:

- The LS (Load share) pins of all modules should be tied together.
- For optimal load sharing, the resistance between the output terminals of each Module to the points where they are all tied together, should be as identical as possible for all modules.
- The Remote Sense lines of all the paralleled Modules should be connected to a single point-of-regulation; all the +SNS lines to one point (if reverse blocking diodes are used, it should be on the cathode side of the diodes) and all the –SNS lines to one point.
- If N+1 redundant configuration is desired (increasing the operational reliability by eliminating single-point failures), or if more than 4 (four) Modules are paralleled, an external reverse blocking diode should be used in series with the +28VDC output of each of the paralleled Modules (see Figure 1). The diodes will prevent a failed Module from overloading the entire 28VDC output. The diode should be able to tolerate the full output current of the Module, at the expected operating temperature.

- Tying together the LS pins of the paralleled Modules allows the BIT circuit of the M7049-103 to detect internal failures that prevent the Module from providing output current, even if the other paralleled Modules are able to support the load and keep the output regulated.

Overload Protection and Input Current

For any given load (Pout) on the 28VDC output, and for any input voltage Vin (the rectified dc voltage at the Module's input), the DC input current into the Module can be estimated using the following formula:

$$I_{IN\text{-}DC} = 1.07 \times Pout / Vin.$$

The RMS current from each of the three phases of the PMG will be approximately: $I_{RMS} = 0.82\ I_{IN\text{-}DC}$

We can see that for any given output power, the loading (in Amps) on the PMG will increase as the PMG voltage decrees. For example, an M7049-103 Module, when operating at 130VDC (about 97Vrms line-to-lime at the PMG output) and loaded by 750W will consume about 6.2Amp from the rectified PMG voltage (about 4.9Arms from each phase of the PMG). At low RPM when the voltage drops to 40VDC (about 31Vrms) the DC input current into the Module will be about 20Amp and the loading on each phase will rise to about 16.5Arms.

Upon request, the M7049 can be factory-configured such that it will prevent the overloading of the PMG at low RPM by reducing the current limit threshold at low input voltage.

Over Voltage Protection.

The M7049-103 contains two independent Over-voltage protection circuits. One is a "smart" electronic circuit that monitors the output voltage and key signals in the Module and in case of an Over-voltage failure of the Module, shuts it down. When a few M7049-103 Modules are paralleled and one of them has an Over-voltage failure, only the Over-voltage protection of the failed Module will trip, and the operation of all other Modules will not be affected. Once tripped, the Module can be reset by toggling its ENABLE signal. The second Over-voltage circuit is a "brute-force" Crowbar across the output terminals of the Module that in case of an irrecoverable failure of the Module, trips and short circuit the 28VDC output. If the failure was caused by a catastrophic short between input to output, the Crowbar will trip an internal fusible link and will disconnect the failed Module from the input source. It should be noted that if a few Modules are connected in parallel without reverse blocking diodes, the Crowbar will short circuit the 28VDC output of all the Modules and will reset only all the ENABLE signals are toggled off.

Over Temperature Protection and Monitor

The Module contains an Over-temperature protection circuit that senses the Module's temperature and disables the Module if it exceeds 95°C (by inadequate cooling). The Module automatically recovers when its temperature drops back below 85°C. In addition, a dedicated temperature sensor (a 10KΩ, logarithmic NTC thermistor, Vishay 2381-640-63103) allows the user to directly monitors of the Module's temperature. The resistance in KΩ as a function of the temperature T in °K is given by the following formula:

$$R = 10*e^{(-14.6337+ 4791.842/T-115334/(T^2) - 3730535/(T^3))}$$

BIT and ENABLE Signals

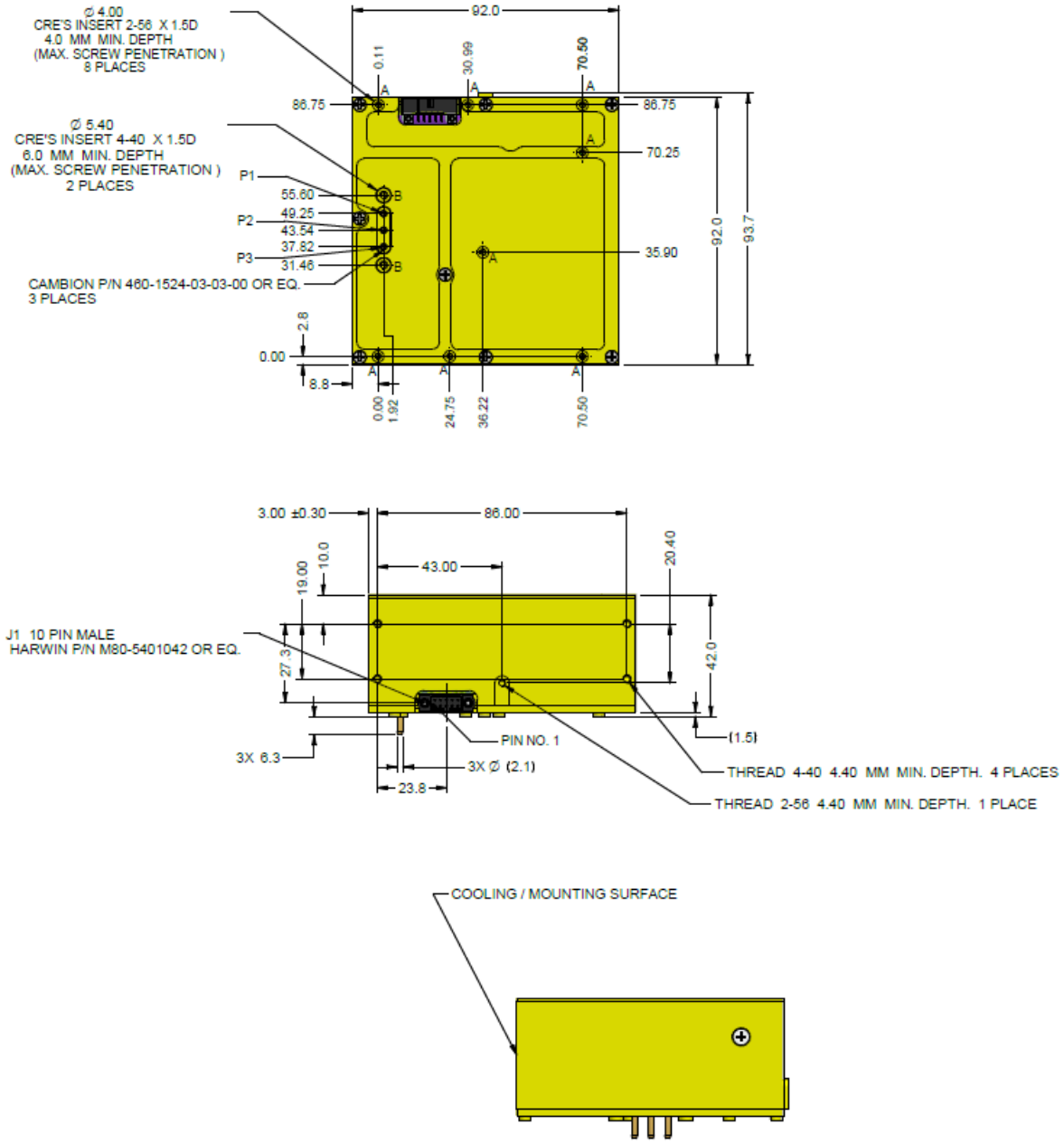
The BIT output of the M7049-103 is the uncommitted output transistor of an opto-coupler (see Fig. 2). The opto-isolation provides the user with the freedom to connect it to any signal-ground and even to connect the BIT signals of a few M7049-103 modules in series with each other (wired AND) or in parallel (wired OR).

The ENABLE input drives the uncommitted input diode (via current limiting resistors and a diode) of an opto-coupler). The ENABLE signal can be provided from any DC source as long that its voltage does not exceed 12VDC and its current does not exceed 15mA. When a common signal source is used to control a few modules, the ENABLE signals can be connected in series or in parallel per the user's preference. Upon request, the ENABLE Logic can be reversed, such that the 28VDC output will be normally On and when voltage is applied to the ENABLE pin(s) the 28VDC output will be disabled (Off).

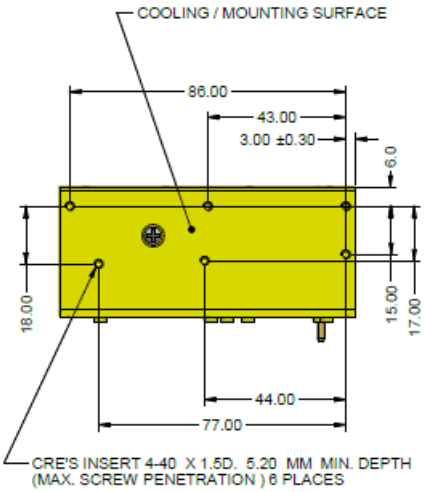
When connecting a few Modules in parallel, maintaining a separate control over the ENABLE signal of each Module, allows the user to test his power system by testing one Module at a time.

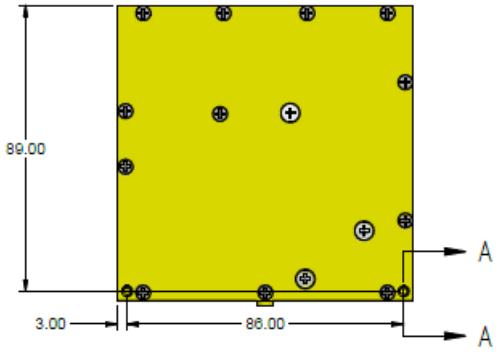
Outline Drawing

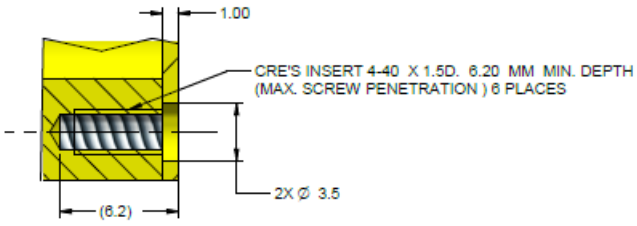
This figure is for reference only. For more details see Drawing M7049003



John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com







Note: Specifications are subject to change without prior notice by the manufacturer

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com