

# 12-CHANNEL RUGGED ETHERNET SWITCH

10/100/1G/2.5G/5G/10GBase-T Compatibility



## DESCRIPTION

Amphenol's 12-channel Rugged Ethernet Switchbox is conduction cooled and configurable for system connectivity, various speeds, port types, as well as interoperation with several high-speed media converters and cable assemblies for system interfacing.

Each copper port is capable of 10/100/1G/2.5G/5G/10GBASE-T Ethernet connectivity. In Amphenol's state of the art communications testing center, the switchbox is aggressively tested at line rates to RFC 2889 for switch and RFC 2544 for L2/L3 performance, latency, packet forwarding and other key items.

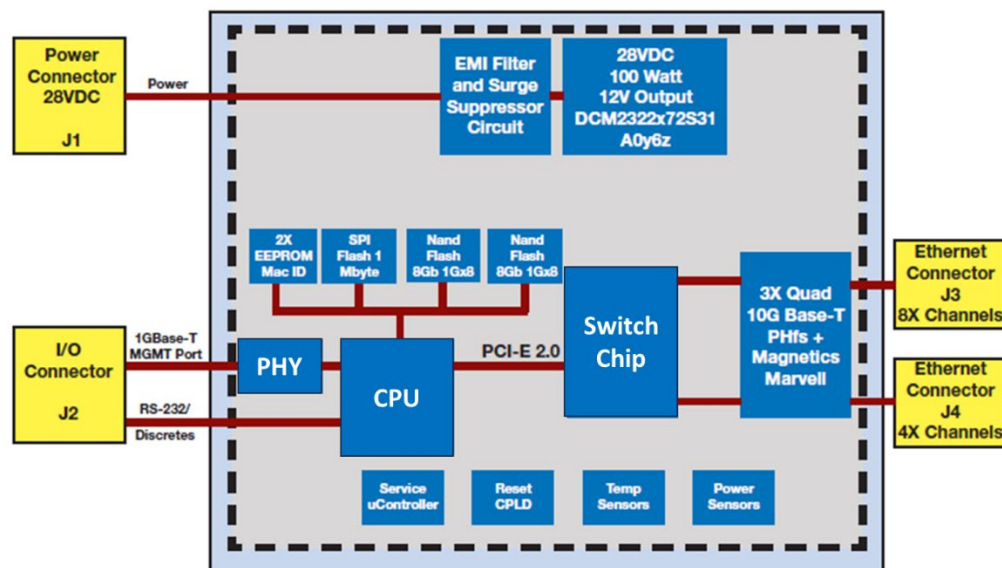
The switch is manufactured using derivatives of Amphenol's MIL-DTL-38999 Series III connectors. These connectors contain standard AS39029 qualified Size 22D contacts and Octonet contacts. Amphenol's Octonet contacts are a proven design used in a variety of military programs. The Octonet is a Size 8 contact that houses four differential pairs, capable of a data rate of 4Gbps maximum and 100Ohm impedance. This contact system has been tested and passed all specification requirements of AS39029 qualification.



## FEATURES AND BENEFITS

- 12-Channels of copper 10/100/1G/2.5G/5G/10GBASE-T
- 28V MIL-STD-740F input module – see this specification for input power considerations.
- 40 watts or less typical power consumption
- Less than 10 second boot time from power on to traffic switching.
- Mil-spec power supply with hold-up capacitor and in-rush current limiting circuit
- Built in test functionality for power up, initiated, and continuous operation.
- MIL-DTL-38999 power, debug/maintenance, and data connectors
- Mil-spec black painted chassis with cold plate external conduction cooling
- Host management process with expanded Ethernet features including:
  - CLI interface and web interface
  - IPV4 / IPV6 routing
  - Information on links and port counters
  - Tagged and untagged vlan configurations
  - Trunk link aggregation
  - Port mirroring
  - Port based QoS
  - 802.1P QoS
  - Rate limitations
  - Loop detection
  - Multicast IGMP snooping
  - Cable diagnostics
  - Access control

## BLOCK DIAGRAM



# SOFTWARE FEATURES

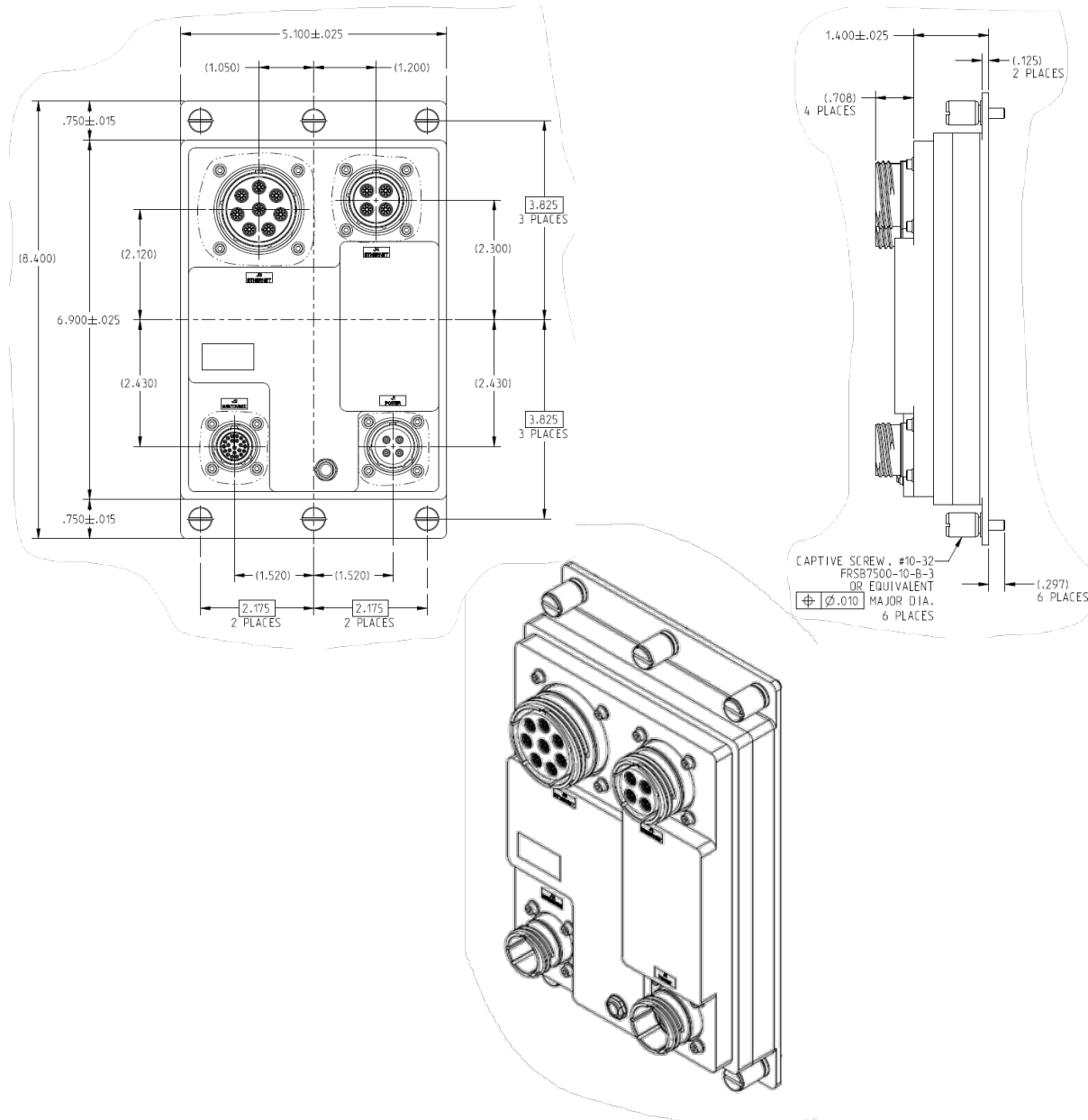
Stacking	Defining IP Addresses	Managing System Files
Stacking Ring Topology	Configuring IP Addressing	Downloading System Files
Stacking Chain Topology	Defining IP Addresses	Firmware Download
Stacking Members and Unit ID	Defining ARP	Configuration Download
Removing and Replacing Stacking Members	Defining Domain Name Servers	Uploading System Files
Exchanging Stacking Members	Defining DNS Servers	Upload Type
Switching the Stacking Master	Defining DNS Host Mapping	Software Image Upload
<b>Configuring System Time</b>	<b>Defining the Forwarding Database</b>	Configuration Upload
Configuring Daylight Savings Time	Defining Static Forwarding Database Entries	Copying Files
Configuring SNTP	Defining Dynamic Forwarding Database Entries	Restoring the Default Configuration File
Polling for Unicast Time Information	<b>Configuring Spanning Tree</b>	<b>Configuring Quality of Service</b>
Polling for Anycast Time Information	Defining Classic Spanning Tree	Quality of Service Overview
Broadcast Time Information	Defining STP on Interfaces	VPT Classification Information
Defining SNTP Settings	Defining Rapid Spanning Tree	CoS Services
<b>Configuring Device Security</b>	Defining Multiple Spanning Tree	Defining General QoS Settings
Configuring Management Security	Defining MSTP Instance Settings	Configuring QoS General Settings
Configuring Authentication Methods	Defining MSTP Interface Settings	Restoring Factory Default QoS Interface Settings
Defining Access Profiles	<b>Configuring SNMP</b>	Defining Queues
Defining Profile Rules	SNMP v1 and v2c	Defining Bandwidth Settings
Defining Authentication Profiles	SNMP v3	Mapping CoS Values to Queues
Mapping Authentication Methods	Configuring SNMP Security	Mapping DSCP Values to Queues
Defining RADIUS Settings	Defining SNMP Security	Defining QoS Basic Mode
Defining TACACS+ Authentication	Defining SNMP View	Defining Basic Mode Settings
Configuring Passwords	Defining SNMP Group Profiles	Rewriting Basic Mode DSCP Values
Defining Local Users	Defining SNMP Group Members	Defining QoS Advanced Mode
Defining Line Passwords	Defining SNMP Communities	Setting Policy Binding
Defining Enable Passwords	SNMP Communities Basic Table	<b>Managing Device Diagnostics</b>
Configuring Network Security	SNMP Communities Advanced Table	Configuring Port Mirroring
Network Security Overview	Configuring SNMP Notifications	<b>Viewing Statistics</b>
Port-Based Authentication	Defining SNMP Notification Global Parameters .	Viewing Interface Statistics
Advanced Port-Based Authentication	Defining SNMP Notification Filters	Viewing Interface Statistics
Defining Port Authentication Properties	Defining SNMP Notification Recipients	Receive Statistics
Defining Port Authentication	SNMPv1,2c Notification Recipients	Transmit Statistics
Configuring Multiple Hosts	SNMPv3 Notification Recipients	Viewing Etherlike Statistics
Defining Authentication Hosts	<b>Configuring Multicast Forwarding</b>	Managing RMON Statistics
Viewing EAP Statistics	Multicast Forwarding	Viewing RMON Statistics
Defining Access Control Lists	Typical Multicast Setup	Configuring RMON History
Defining IP Based Access Control Lists	Multicast Operation	Defining RMON History Control
Defining MAC Based Access Control Lists	Multicast Registration	Viewing the RMON History Table
Binding Device Security ACLs	Multicast Address Properties	Configuring RMON Events
Managing Port Security	Defining Multicast Properties	Defining RMON Events Control
Enabling Storm Control	Adding MAC Group Address	Viewing the RMON Events Logs
<b>Configuring System Logs</b>	Adding IP Multicast Groups	Defining RMON Alarms
Defining General Log Properties	Configuring IGMP Snooping	
Viewing Memory Logs	Configuring MLD Snooping	
Viewing Flash Logs	Viewing IGMP/MLD IP Multicast Groups	
<b>Configuring Interfaces</b>	Defining Multicast Router Ports	
Configuring Ports	Defining Forward All Multicast	
Aggregating Ports	Defining Unregistered Multicast Settings	
Configuring LACP		
Configuring VLANs		
Defining VLAN Properties		
Defining VLAN Membership		
Defining VLAN Interface Settings		
Configuring GARP		
Defining GARP		
Defining GVRP		
Viewing GVRP Statistics		

## ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CF-020400-076	12-channel rugged network switch, 12x 10/100/1G/2.5G/5G/10GBASE-T

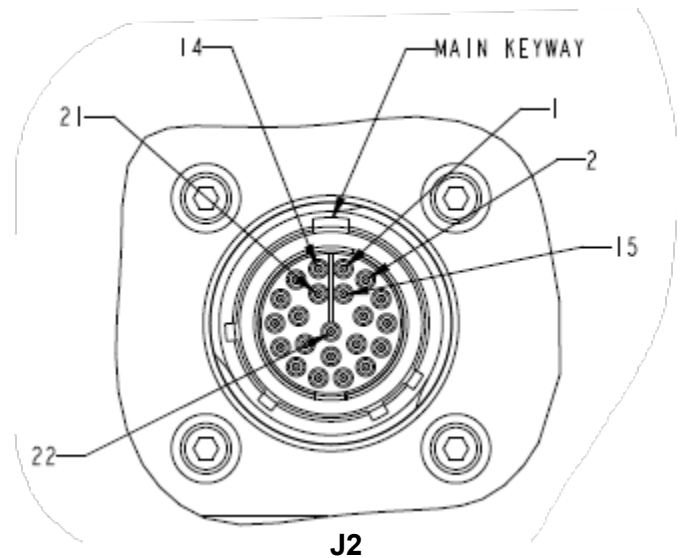
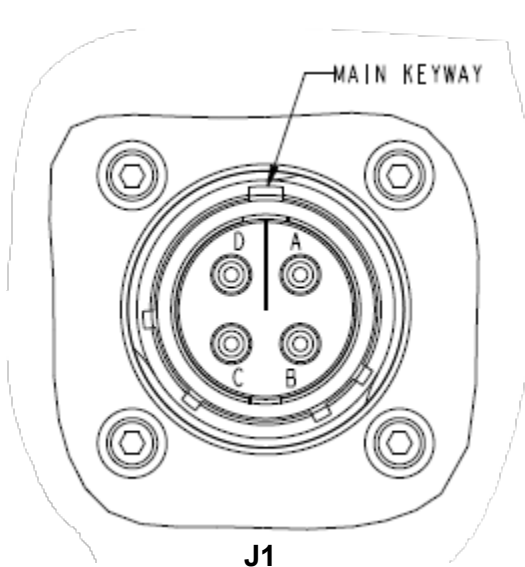
## MECHANICAL SPECIFICATIONS

CF-020400-076

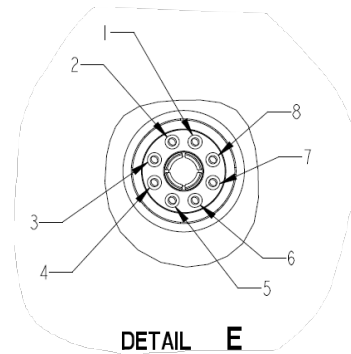
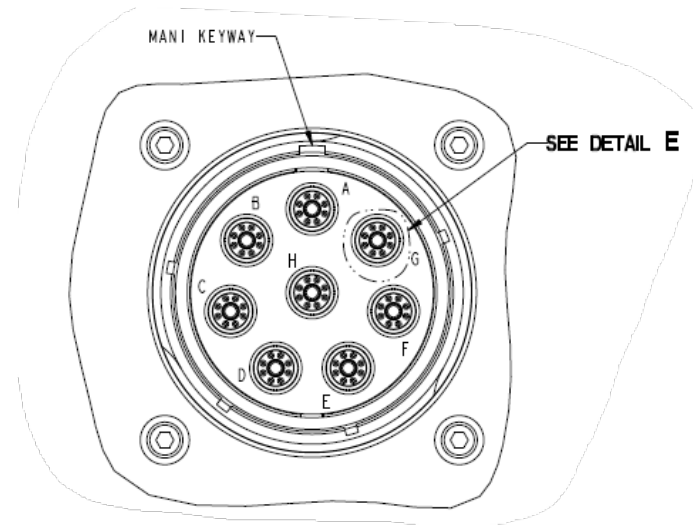


CF-020400-076 PINOUT

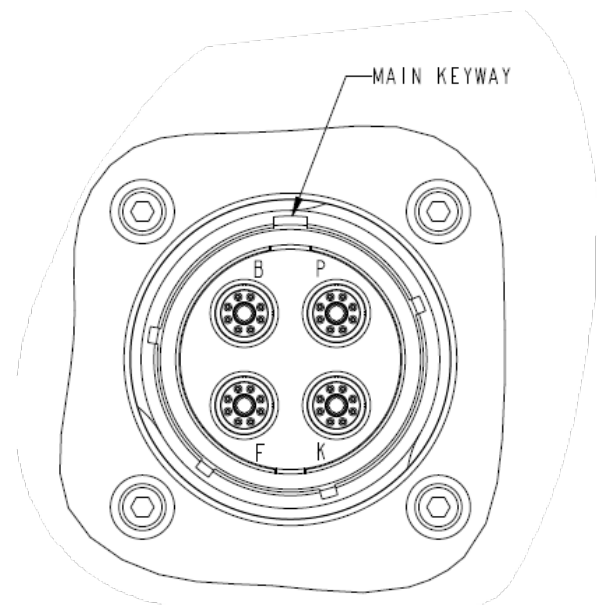
I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P	A	IN	280VDC_IN
	B	OUT	28VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J2 (MAINTENANCE) 13-35P	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	OUT	POWER_SUPPLY_STATUS
	5	IN	RS232_PIC_RX
	6	OUT	RS232_PIC_TX
	7	OUT	CHASSIS_STATUS
	8	--	RS232_PIC_GND
	9	OUT	TEMP_WARNING_STATUS
	10	BI	DEBUG_I2C_SCL
	11	BI	DEBUG_I2C_SDA
	12	--	RESET
	13	--	RESET_RETURN
	14	BI	DEBUG_CPU_1GBASET_DA+
	15		DEBUG_CPU_1GBASET_DA-
	16		DEBUG_CPU_1GBASET_DB+
	17		DEBUG_CPU_1GBASET_DB-
	18		DEBUG_CPU_1GBASET_DC+
	19		DEBUG_CPU_1GBASET_DC-
	20	DEBUG_CPU_1GBASET_DD+	
	21	DEBUG_CPU_1GBASET_DD-	
	22	--	NOT CONNECTED
SHELL	--	CHASSIS	



I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3 10GBASE-T 25-8S	A-1	BI	PORT1_10GBASE-T_DA+
	A-2		PORT1_10GBASE-T_DA-
	A-3		PORT1_10GBASE-T_DB+
	A-4		PORT1_10GBASE-T_DB-
	A-5		PORT1_10GBASE-T_DC+
	A-6		PORT1_10GBASE-T_DC-
	A-7		PORT1_10GBASE-T_DD+
	A-8		PORT1_10GBASE-T_DD-
	A-OUTER		CHASSIS
	B-1	BI	PORT2_10GBASE-T_DA+
	B-2		PORT2_10GBASE-T_DA-
	B-3		PORT2_10GBASE-T_DB+
	B-4		PORT2_10GBASE-T_DB-
	B-5		PORT2_10GBASE-T_DC+
	B-6		PORT2_10GBASE-T_DC-
	B-7		PORT2_10GBASE-T_DD+
	B-8		PORT2_10GBASE-T_DD-
	B-OUTER		CHASSIS
	C-1	BI	PORT3_10GBASE-T_DA+
	C-2		PORT3_10GBASE-T_DA-
	C-3		PORT3_10GBASE-T_DB+
	C-4		PORT3_10GBASE-T_DB-
	C-5		PORT3_10GBASE-T_DC+
	C-6		PORT3_10GBASE-T_DC-
	C-7		PORT3_10GBASE-T_DD+
	C-8		PORT3_10GBASE-T_DD-
	C-OUTER		CHASSIS
	D-1	BI	PORT4_10GBASE-T_DA+
	D-2		PORT4_10GBASE-T_DA-
	D-3		PORT4_10GBASE-T_DB+
	D-4		PORT4_10GBASE-T_DB-
	D-5		PORT4_10GBASE-T_DC+
	D-6		PORT4_10GBASE-T_DC-
	D-7		PORT4_10GBASE-T_DD+
	D-8		PORT4_10GBASE-T_DD-
	D-OUTER		CHASSIS
	E-1	BI	PORT5_10GBASE-T_DA+
	E-2		PORT5_10GBASE-T_DA-
	E-3		PORT5_10GBASE-T_DB+
	E-4		PORT5_10GBASE-T_DB-
E-5	PORT5_10GBASE-T_DC+		
E-6	PORT5_10GBASE-T_DC-		
E-7	PORT5_10GBASE-T_DD+		
E-8	PORT5_10GBASE-T_DD-		
E-OUTER		CHASSIS	
F-1	BI	PORT6_10GBASE-T_DA+	
F-2		PORT6_10GBASE-T_DA-	
F-3		PORT6_10GBASE-T_DB+	
F-4		PORT6_10GBASE-T_DB-	
F-5		PORT6_10GBASE-T_DC+	
F-6		PORT6_10GBASE-T_DC-	
F-7		PORT6_10GBASE-T_DD+	
F-8		PORT6_10GBASE-T_DD-	
F-OUTER		CHASSIS	



I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3 10GBASE-T 25-8S	G-1	BI	PORT7_10GBASE-T_DA+
	G-2		PORT7_10GBASE-T_DA-
	G-3		PORT7_10GBASE-T_DB+
	G-4		PORT7_10GBASE-T_DB-
	G-5		PORT7_10GBASE-T_DC+
	G-6		PORT7_10GBASE-T_DC-
	G-7		PORT7_10GBASE-T_DD+
	G-8		PORT7_10GBASE-T_DD-
	G-OUTER		CHASSIS
	H-1	BI	PORT8_10GBASE-T_DA+
	H-2		PORT8_10GBASE-T_DA-
	H-3		PORT8_10GBASE-T_DB+
	H-4		PORT8_10GBASE-T_DB-
	H-5		PORT8_10GBASE-T_DC+
	H-6		PORT8_10GBASE-T_DC-
	H-7		PORT8_10GBASE-T_DD+
	H-8		PORT8_10GBASE-T_DD-
H-OUTER		CHASSIS	
SHELL	--	CHASSIS	
J4 10GBASE-T 19-ABS	B-1	BI	PORT9_10GBASE-T_DA+
	B-2		PORT9_10GBASE-T_DA-
	B-3		PORT9_10GBASE-T_DB+
	B-4		PORT9_10GBASE-T_DB-
	B-5		PORT9_10GBASE-T_DC+
	B-6		PORT9_10GBASE-T_DC-
	B-7		PORT9_10GBASE-T_DD+
	B-8		PORT9_10GBASE-T_DD-
	B-OUTER		CHASSIS
	F-1	BI	PORT10_10GBASE-T_DA+
	F-2		PORT10_10GBASE-T_DA-
	F-3		PORT10_10GBASE-T_DB+
	F-4		PORT10_10GBASE-T_DB-
	F-5		PORT10_10GBASE-T_DC+
	F-6		PORT10_10GBASE-T_DC-
	F-7		PORT10_10GBASE-T_DD+
	F-8		PORT10_10GBASE-T_DD-
	F-OUTER		CHASSIS
	K-1	BI	PORT11_10GBASE-T_DA+
	K-2		PORT11_10GBASE-T_DA-
	K-3		PORT11_10GBASE-T_DB+
	K-4		PORT11_10GBASE-T_DB-
	K-5		PORT11_10GBASE-T_DC+
	K-6		PORT11_10GBASE-T_DC-
K-7	PORT11_10GBASE-T_DD+		
K-8	PORT11_10GBASE-T_DD-		
K-OUTER		CHASSIS	
P-1	BI	PORT12_10GBASE-T_DA+	
P-2		PORT12_10GBASE-T_DA-	
P-3		PORT12_10GBASE-T_DB+	
P-4		PORT12_10GBASE-T_DB-	
P-5		PORT12_10GBASE-T_DC+	
P-6		PORT12_10GBASE-T_DC-	
P-7		PORT12_10GBASE-T_DD+	
P-8		PORT12_10GBASE-T_DD-	
P-OUTER		CHASSIS	
SHELL	--	CHASSIS	



# Amphenol Ruggedization Design

## OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

## TEMPERATURE:

- Operating Temperature
  - Thermal Cycles between -40°C and 85°C while device is operating
- Temperature is measured at chassis housing or card edge
  - Storage Temperature- Thermal Cycles between -55°C and 125°C

## HUMIDITY:

- Operating Humidity
  - Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity
  - Humidity cycle between 0-100% condensing humidity

## SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10<sup>-5</sup> cc/sec performance

## SHOCK AND VIBRATION:

- Sine Vibration
  - PORT1\_10G Peak, 5-2,000Hz
  - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration
  - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
  - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
  - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

## FLUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

## ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

## ELECTROMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

## PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
  - Amphenol performs Conformal Coating to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
  - Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
  - Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

## OTHER:

- Designed for MIL-STD-704F Power
- Salt/Fog/Dust
- Fluids and Rain
- Explosive atmosphere

## RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL-HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method.



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40-60 Delaware Avenue

Sidney, NY 13838

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