Amphenol
MILITARY HIGH SPEED

120 CHANNEL ETHERNET SWITCH

RUGGEDIZED ETHERNET SWITCHBOX

CF-020011-433

DESCRIPTION

Amphenol's Rugged 120 Channel Ethernet Switch Box provides an unmatched level of flexibility to meet any system requirement. The switch box is a 120 port standalone Ethernet Switch box that is configurable for system connectivity, speeds, port types, and interoperation with various high-speed media converters and connectors for system interfacing.

Each port is capable of 10G Ethernet – some ports can either be configured as 10G-Base-T (also supporting 100-Base-T and 1G-Base-T) or 10G-Base-SR and 1G-Base-SX. The switching throughput is up to 1.2 Tbps when using all 120 ports on the switch box. In addition, the switch is non-blocking and low-latency for high-throughput architectures and applications. In Amphenol's state of the art Spirent communications testing center, the switch box is tested aggressively at line rates to RFC 2889 for switching and RFC 2544 for L2/L3 performance, latency, packet forwarding, and other key items.

The switch is manufactured using Amphenol's MIL Qualified MIL-DTL-38999 Series III connectors. These connectors contain standard AS39029 qualified Size 22D contacts, Octonet contacts and 48F MT Ferrule Fiber Optic contact assemblies.

Amphenol's Octonet Contacts are a proven design used in a variety of Military Programs. The Octonet is a Size 8 contact housing (4) differential pair contacts. It is a 100 Ohm impedance, capable of a data rate of 4 Gbps maximum per contact pair. The contact system has been tested and passed all the Qualification Requirements of AS39029 contacts.

Our 48F MT Ferrule Fiber Optic Contacts are industry standard, very high density plastic ferrules available in either 12-fiber, 24-fiber versions, 48 pin, in multi-mode PC, single mode PC, or single mode APC configurations.

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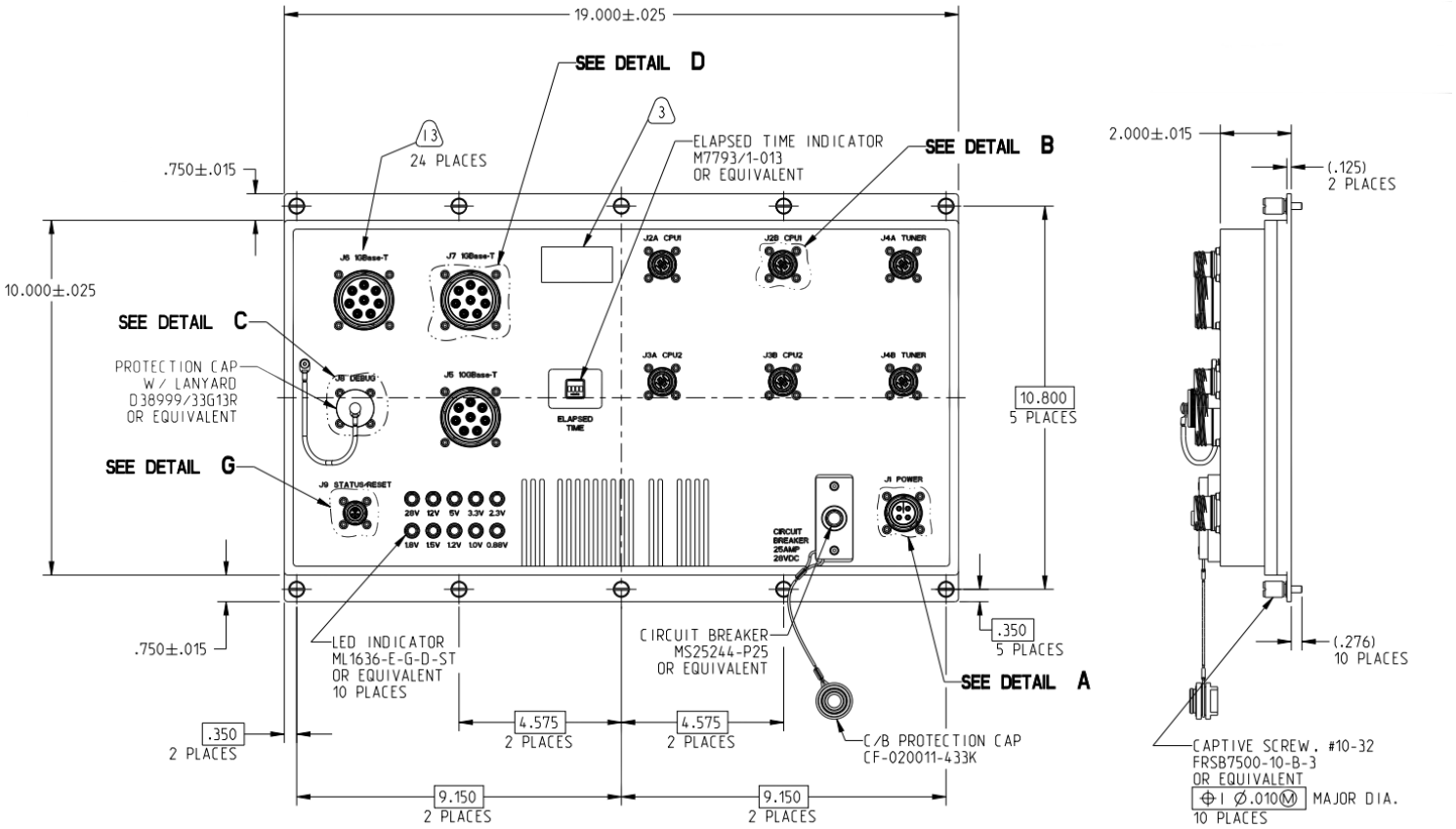
FEATURES & BENEFITS:

- 96 ports of 10GBASE-SR (Can also be configured for 1GBase-SX)
- 24 ports of 100/1G/10GBase-T - auto negotiation
- Supports Ethernet multicast, IP multicast, GMP, SNMP, & many other management options
- Host management processor
- Chassis with 38999 series III high performance & density connectors
- 10 LED indicators reporting all internal power supply voltage levels
- MIL-STD-704 28V DC power supply interface
- 50ms power holdup
- Embedded elapsed time indicator
- Circuit breaker for incoming power
- Self-encapsulated mounting screws
- -55 C to 85 C operating depending on altitude – perfect for military aerospace environments
- Conduction cooled for cold plate interface
- Vita 47 Shock and Vibration
- Plating & paint is configurable
- EMI/EMC per MIL-STD-461 E

DIMENTIONAL INFORMATION:



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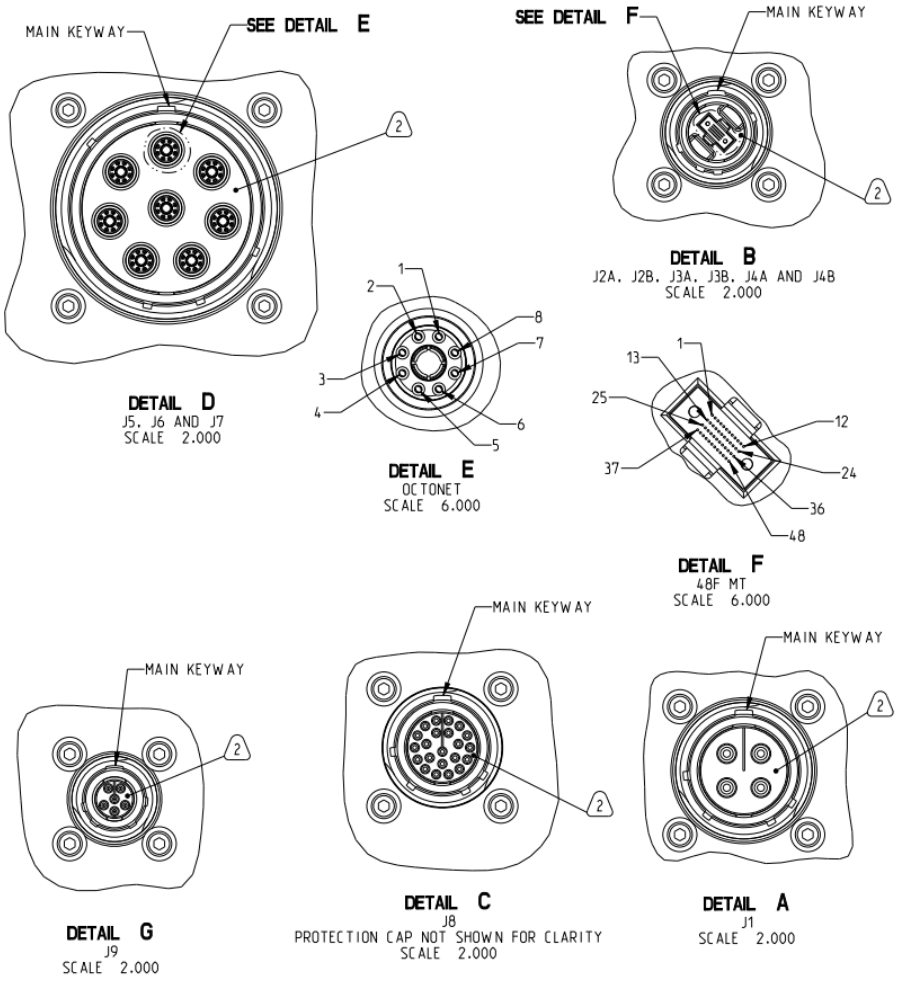

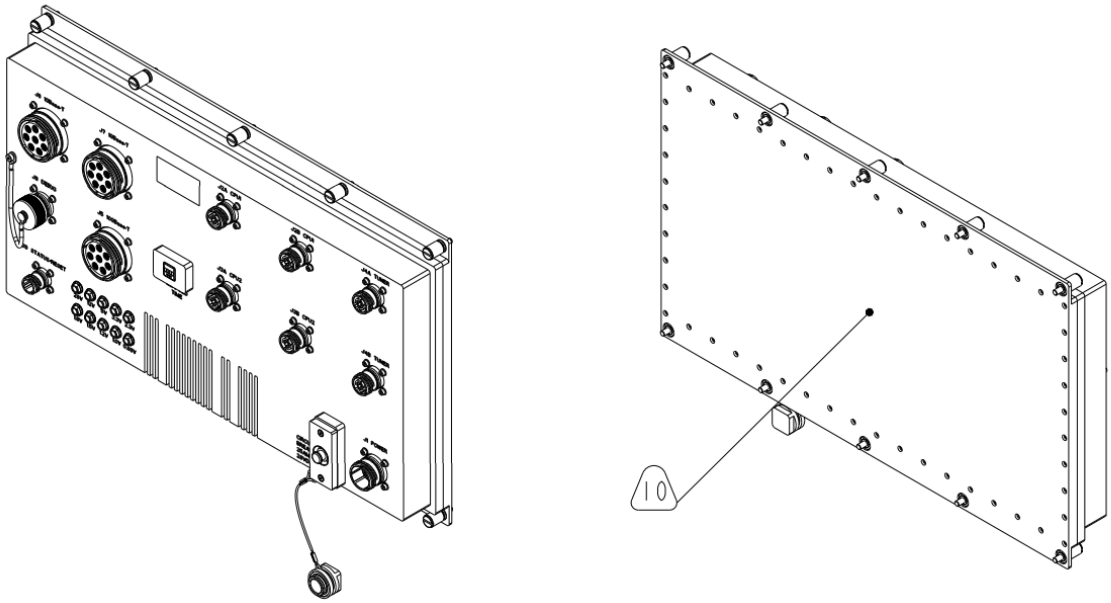

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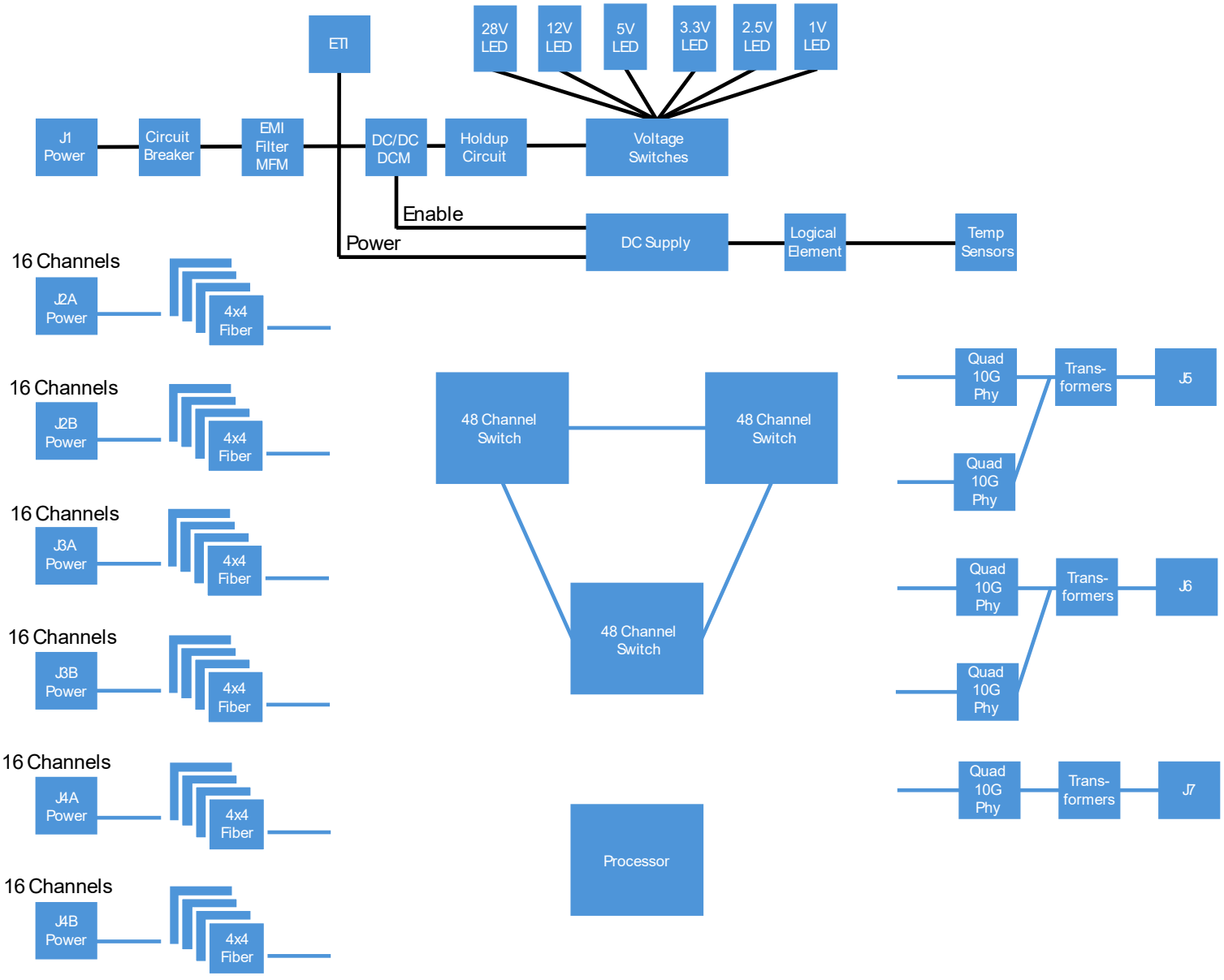
BLOCK DIAGRAM:



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I/O CHARTS:

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	28VDC_IN
	B	OUT	28VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J8 (DEBUG) 13-35P KEYING "N" WITH METAL CAP	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	IN	DEBUG_JTAG_TCLK
	5	OUT	DEBUG_JTAG_TDO
	6	IN	DEBUG_JTAG_TDI
	7	IN	DEBUG_JTAG_TTMS
	8	IN	DEBUG_I2C_SCL
	9	BI	DEBUG_I2C_SDA
	10	--	NOT CONNECTED
	11	--	NOT CONNECTED
	12	BI	DEBUG_CPU_USB_D+
	13	BI	DEBUG_CPU_USB_D-
	14	BI	DEBUG_CPU_1GBASET_DA+
	15		DEBUG_CPU_1GBASET_DA-
	16		DEBUG_CPU_1GBASET_DB+
	17		DEBUG_CPU_1GBASET_DB-
	18		DEBUG_CPU_1GBASET_DC+
	19		DEBUG_CPU_1GBASET_DC-
	20		DEBUG_CPU_1GBASET_DD+
	21		DEBUG_CPU_1GBASET_DD-
	22	--	NOT CONNECTED
	SHELL	--	CHASSIS
J9 (STATUS/RESET) 9-35P KEYING "N"	1	IN	SWITCHBOX_RESET
	2	OUT	POWERSUPPLY_STATUS
	3	OUT	CHASSIS_STATUS
	4	OUT	TEMPERATURE_WARNING_STATUS
	5	--	RESET_RTN
	6	--	NOT CONNECTED
	SHELL	--	CHASSIS

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2A (CPU1) 11-1S 48F MT KEYING "N"	1	OUT	PORT1_10GBASESR_TX
	2		PORT2_10GBASESR_TX
	3		PORT3_10GBASESR_TX
	4		PORT4_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT4_10GBASESR_RX
	10		PORT3_10GBASESR_RX
	11		PORT2_10GBASESR_RX
	12		PORT1_10GBASESR_RX
	13	OUT	PORT5_10GBASESR_TX
	14		PORT6_10GBASESR_TX
	15		PORT7_10GBASESR_TX
	16		PORT8_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT8_10GBASESR_RX
	22		PORT7_10GBASESR_RX
	23		PORT6_10GBASESR_RX
	24		PORT5_10GBASESR_RX
	25	OUT	PORT9_1GBASESX_TX
	26		PORT10_1GBASESX_TX
	27		PORT11_1GBASESX_TX
	28		PORT12_1GBASESX_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT12_1GBASESX_RX
	34		PORT11_1GBASESX_RX
	35		PORT10_1GBASESX_RX
	36		PORT9_1GBASESX_RX
	37	OUT	PORT13_1GBASESX_TX
	38		PORT14_1GBASESX_TX
	39		PORT15_1GBASESX_TX
	40		PORT16_1GBASESX_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT16_1GBASESX_RX
	46		PORT15_1GBASESX_RX
	47		PORT14_1GBASESX_RX
	48		PORT13_1GBASESX_RX
	SHELL	--	CHASSIS

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I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2B (CPU1) 11-1S 48F MT KEYING "A"	1	OUT	PORT17_10GBASESR_TX
	2		PORT18_10GBASESR_TX
	3		PORT19_10GBASESR_TX
	4		PORT20_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT20_10GBASESR_RX
	10		PORT19_10GBASESR_RX
	11		PORT18_10GBASESR_RX
	12		PORT17_10GBASESR_RX
	13	OUT	PORT21_10GBASESR_TX
	14		PORT22_10GBASESR_TX
	15		PORT23_10GBASESR_TX
	16		PORT24_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT24_10GBASESR_RX
	22		PORT23_10GBASESR_RX
	23		PORT22_10GBASESR_RX
	24		PORT21_10GBASESR_RX
	25	OUT	PORT25_1GBASESX_TX
	26		PORT26_1GBASESX_TX
	27		PORT27_1GBASESX_TX
	28		PORT28_1GBASESX_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT28_1GBASESX_RX
	34		PORT27_1GBASESX_RX
	35		PORT26_1GBASESX_RX
	36		PORT25_1GBASESX_RX
	37	OUT	PORT29_1GBASESX_TX
	38		PORT30_1GBASESX_TX
	39		PORT31_1GBASESX_TX
	40		PORT32_1GBASESX_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT32_1GBASESX_RX
	46		PORT31_1GBASESX_RX
	47		PORT30_1GBASESX_RX
	48		PORT29_1GBASESX_RX
	SHELL	--	CHASSIS

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3A (CPU2) 11-1S 48F MT KEYING "B"	1	OUT	PORT33_10GBASESR_TX
	2		PORT34_10GBASESR_TX
	3		PORT35_10GBASESR_TX
	4		PORT36_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT36_10GBASESR_RX
	10		PORT35_10GBASESR_RX
	11		PORT34_10GBASESR_RX
	12		PORT33_10GBASESR_RX
	13	OUT	PORT37_10GBASESR_TX
	14		PORT38_10GBASESR_TX
	15		PORT39_10GBASESR_TX
	16		PORT40_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT40_10GBASESR_RX
	22		PORT39_10GBASESR_RX
	23		PORT38_10GBASESR_RX
	24		PORT37_10GBASESR_RX
	25	OUT	PORT41_1GBASESX_TX
	26		PORT42_1GBASESX_TX
	27		PORT43_1GBASESX_TX
	28		PORT44_1GBASESX_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT44_1GBASESX_RX
	34		PORT43_1GBASESX_RX
	35		PORT42_1GBASESX_RX
	36		PORT41_1GBASESX_RX
	37	OUT	PORT45_1GBASESX_TX
	38		PORT46_1GBASESX_TX
	39		PORT47_1GBASESX_TX
	40		PORT48_1GBASESX_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT48_1GBASESX_RX
	46		PORT47_1GBASESX_RX
	47		PORT46_1GBASESX_RX
	48		PORT45_1GBASESX_RX
	SHELL	--	CHASSIS

I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3B (CPU2) 11-1S 48F MT KEYING "C"	1	OUT	PORT49_10GBASESR_TX
	2		PORT50_10GBASESR_TX
	3		PORT51_10GBASESR_TX
	4		PORT52_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT52_10GBASESR_RX
	10		PORT51_10GBASESR_RX
	11		PORT50_10GBASESR_RX
	12		PORT49_10GBASESR_RX
	13	OUT	PORT53_10GBASESR_TX
	14		PORT54_10GBASESR_TX
	15		PORT55_10GBASESR_TX
	16		PORT56_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT56_10GBASESR_RX
	22		PORT55_10GBASESR_RX
	23		PORT54_10GBASESR_RX
	24		PORT53_10GBASESR_RX
	25	OUT	PORT57_1GBASESX_TX
	26		PORT58_1GBASESX_TX
	27		PORT59_1GBASESX_TX
	28		PORT60_1GBASESX_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT60_1GBASESX_RX
	34		PORT59_1GBASESX_RX
	35		PORT58_1GBASESX_RX
	36		PORT57_1GBASESX_RX
	37	OUT	PORT61_1GBASESX_TX
	38		PORT62_1GBASESX_TX
	39		PORT63_1GBASESX_TX
	40		PORT64_1GBASESX_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT64_1GBASESX_RX
	46		PORT63_1GBASESX_RX
	47		PORT62_1GBASESX_RX
	48		PORT61_1GBASESX_RX
	SHELL	--	CHASSIS

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J4A (TUNER) 11-1S 48F MT KEYING "D"	1	OUT	PORT65_10GBASESR_TX
	2		PORT66_10GBASESR_TX
	3		PORT67_10GBASESR_TX
	4		PORT68_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT68_10GBASESR_RX
	10		PORT67_10GBASESR_RX
	11		PORT66_10GBASESR_RX
	12		PORT65_10GBASESR_RX
	13	OUT	PORT69_10GBASESR_TX
	14		PORT70_10GBASESR_TX
	15		PORT71_10GBASESR_TX
	16		PORT72_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT72_10GBASESR_RX
	22		PORT71_10GBASESR_RX
	23		PORT70_10GBASESR_RX
	24		PORT69_10GBASESR_RX
	25	OUT	PORT73_10GBASESR_TX
	26		PORT74_10GBASESR_TX
	27		PORT75_1GBASESX_TX
	28		PORT76_1GBASESX_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT76_1GBASESX_RX
	34		PORT75_1GBASESX_RX
	35		PORT74_10GBASESR_RX
	36		PORT73_10GBASESR_RX
	37	OUT	PORT77_1GBASESX_TX
	38		PORT78_1GBASESX_TX
	39		PORT79_1GBASESX_TX
	40		PORT80_1GBASESX_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT80_1GBASESX_RX
	46		PORT79_1GBASESX_RX
	47		PORT78_1GBASESX_RX
	48		PORT77_1GBASESX_RX
	SHELL	--	CHASSIS

I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J4B (TUNER) 11-1S 48F MT KEYING "E"	1	OUT	PORT81_10GBASESR_TX
	2		PORT82_10GBASESR_TX
	3		PORT83_10GBASESR_TX
	4		PORT84_10GBASESR_TX
	5-8	--	NOT CONNECTED
	9	IN	PORT84_10GBASESR_RX
	10		PORT83_10GBASESR_RX
	11		PORT82_10GBASESR_RX
	12		PORT81_10GBASESR_RX
	13	OUT	PORT85_10GBASESR_TX
	14		PORT86_10GBASESR_TX
	15		PORT87_10GBASESR_TX
	16		PORT88_10GBASESR_TX
	17-20	--	NOT CONNECTED
	21	IN	PORT88_10GBASESR_RX
	22		PORT87_10GBASESR_RX
	23		PORT86_10GBASESR_RX
	24		PORT85_10GBASESR_RX
	25	OUT	PORT89_10GBASESR_TX
	26		PORT90_10GBASESR_TX
	27		PORT91_10GBASESR_TX
	28		PORT92_10GBASESR_TX
	29-32	--	NOT CONNECTED
	33	IN	PORT92_10GBASESR_RX
	34		PORT91_10GBASESR_RX
	35		PORT90_10GBASESR_RX
	36		PORT89_10GBASESR_RX
	37	OUT	PORT93_10GBASESR_TX
	38		PORT94_10GBASESR_TX
	39		PORT95_10GBASESR_TX
	40		PORT96_10GBASESR_TX
	41-44	--	NOT CONNECTED
	45	IN	PORT96_10GBASESR_RX
	46		PORT95_10GBASESR_RX
	47		PORT94_10GBASESR_RX
	48		PORT93_10GBASESR_RX
	SHELL	--	CHASSIS

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J5 (10GBASE-T) 25-8S KEYING "N"	A-1	BI	PORT97_10GBASET_DA+
	A-2		PORT97_10GBASET_DA-
	A-3		PORT97_10GBASET_DB+
	A-4		PORT97_10GBASET_DB-
	A-5		PORT97_10GBASET_DC+
	A-6		PORT97_10GBASET_DC-
	A-7		PORT97_10GBASET_DD+
	A-8		PORT97_10GBASET_DD-
	B-1		PORT98_10GBASET_DA+
	B-2		PORT98_10GBASET_DA-
	B-3		PORT98_10GBASET_DB+
	B-4		PORT98_10GBASET_DB-
	B-5		PORT98_10GBASET_DC+
	B-6		PORT98_10GBASET_DC-
	B-7		PORT98_10GBASET_DD+
	B-8		PORT98_10GBASET_DD-
	C-1		PORT99_10GBASET_DA+
	C-2		PORT99_10GBASET_DA-
	C-3		PORT99_10GBASET_DB+
	C-4		PORT99_10GBASET_DB-
	C-5		PORT99_10GBASET_DC+
	C-6		PORT99_10GBASET_DC-
	C-7		PORT99_10GBASET_DD+
	C-8		PORT99_10GBASET_DD-
	D-1		PORT100_10GBASET_DA+
	D-2		PORT100_10GBASET_DA-
	D-3		PORT100_10GBASET_DB+
	D-4		PORT100_10GBASET_DB-
	D-5		PORT100_10GBASET_DC+
	D-6		PORT100_10GBASET_DC-
	D-7		PORT100_10GBASET_DD+
	D-8		PORT100_10GBASET_DD-

I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J5 (10GBASE-T) 25-8S KEYING "N"	E-1	BI	PORT101_10GBASET_DA+
	E-2		PORT101_10GBASET_DA-
	E-3		PORT101_10GBASET_DB+
	E-4		PORT101_10GBASET_DB-
	E-5		PORT101_10GBASET_DC+
	E-6		PORT101_10GBASET_DC-
	E-7		PORT101_10GBASET_DD+
	E-8		PORT101_10GBASET_DD-
	F-1		PORT102_10GBASET_DA+
	F-2		PORT102_10GBASET_DA-
	F-3		PORT102_10GBASET_DB+
	F-4		PORT102_10GBASET_DB-
	F-5		PORT102_10GBASET_DC+
	F-6		PORT102_10GBASET_DC-
	F-7		PORT102_10GBASET_DD+
	F-8		PORT102_10GBASET_DD-
	G-1		PORT103_10GBASET_DA+
	G-2		PORT103_10GBASET_DA-
	G-3		PORT103_10GBASET_DB+
	G-4		PORT103_10GBASET_DB-
	G-5		PORT103_10GBASET_DC+
	G-6		PORT103_10GBASET_DC-
	G-7		PORT103_10GBASET_DD+
	G-8		PORT103_10GBASET_DD-
	H-1		PORT104_10GBASET_DA+
	H-2		PORT104_10GBASET_DA-
	H-3		PORT104_10GBASET_DB+
	H-4		PORT104_10GBASET_DB-
	H-5		PORT104_10GBASET_DC+
	H-6		PORT104_10GBASET_DC-
	H-7		PORT104_10GBASET_DD+
	H-8		PORT104_10GBASET_DD-
	A OUTER	--	CHASSIS
	B OUTER		
	C OUTER		
	D OUTER		
	E OUTER		
	F OUTER		
	G OUTER		
	H OUTER		
	SHELL		

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J6 (1GBASE-T) 25-8S KEYING "A"	A-1	BI	PORT105_1GBASET_DA+
	A-2		PORT105_1GBASET_DA-
	A-3		PORT105_1GBASET_DB+
	A-4		PORT105_1GBASET_DB-
	A-5		PORT105_1GBASET_DC+
	A-6		PORT105_1GBASET_DC-
	A-7		PORT105_1GBASET_DD+
	A-8		PORT105_1GBASET_DD-
	B-1		PORT106_1GBASET_DA+
	B-2		PORT106_1GBASET_DA-
	B-3		PORT106_1GBASET_DB+
	B-4		PORT106_1GBASET_DB-
	B-5		PORT106_1GBASET_DC+
	B-6		PORT106_1GBASET_DC-
	B-7		PORT106_1GBASET_DD+
	B-8		PORT106_1GBASET_DD-
	C-1		PORT107_1GBASET_DA+
	C-2		PORT107_1GBASET_DA-
	C-3		PORT107_1GBASET_DB+
	C-4		PORT107_1GBASET_DB-
	C-5		PORT107_1GBASET_DC+
	C-6		PORT107_1GBASET_DC-
	C-7		PORT107_1GBASET_DD+
	C-8		PORT107_1GBASET_DD-
	D-1		PORT108_1GBASET_DA+
	D-2		PORT108_1GBASET_DA-
	D-3		PORT108_1GBASET_DB+
	D-4		PORT108_1GBASET_DB-
	D-5		PORT108_1GBASET_DC+
	D-6		PORT108_1GBASET_DC-
	D-7		PORT108_1GBASET_DD+
	D-8		PORT108_1GBASET_DD-

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I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J6 (1GBASE-T) 25-8S KEYING "A"	E-1	BI	PORT109_1GBASET_DA+
	E-2		PORT109_1GBASET_DA-
	E-3		PORT109_1GBASET_DB+
	E-4		PORT109_1GBASET_DB-
	E-5		PORT109_1GBASET_DC+
	E-6		PORT109_1GBASET_DC-
	E-7		PORT109_1GBASET_DD+
	E-8		PORT109_1GBASET_DD-
	F-1		PORT110_1GBASET_DA+
	F-2		PORT110_1GBASET_DA-
	F-3		PORT110_1GBASET_DB+
	F-4		PORT110_1GBASET_DB-
	F-5		PORT110_1GBASET_DC+
	F-6		PORT110_1GBASET_DC-
	F-7		PORT110_1GBASET_DD+
	F-8		PORT110_1GBASET_DD-
	G-1		PORT111_1GBASET_DA+
	G-2		PORT111_1GBASET_DA-
	G-3		PORT111_1GBASET_DB+
	G-4		PORT111_1GBASET_DB-
	G-5		PORT111_1GBASET_DC+
	G-6		PORT111_1GBASET_DC-
	G-7		PORT111_1GBASET_DD+
	G-8		PORT111_1GBASET_DD-
	H-1		PORT112_1GBASET_DA+
	H-2		PORT112_1GBASET_DA-
	H-3		PORT112_1GBASET_DB+
	H-4		PORT112_1GBASET_DB-
	H-5		PORT112_1GBASET_DC+
	H-6		PORT112_1GBASET_DC-
	H-7		PORT112_1GBASET_DD+
	H-8		PORT112_1GBASET_DD-
	A OUTER	--	CHASSIS
	B OUTER		
	C OUTER		
	D OUTER		
	E OUTER		
	F OUTER		
	G OUTER		
	H OUTER		
	SHELL		

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J7 (1GBASE-T) 25-8S KEYING "B"	A-1	BI	PORT113_1GBASET_DA+
	A-2		PORT113_1GBASET_DA-
	A-3		PORT113_1GBASET_DB+
	A-4		PORT113_1GBASET_DB-
	A-5		PORT113_1GBASET_DC+
	A-6		PORT113_1GBASET_DC-
	A-7		PORT113_1GBASET_DD+
	A-8		PORT113_1GBASET_DD-
	B-1		PORT114_1GBASET_DA+
	B-2		PORT114_1GBASET_DA-
	B-3		PORT114_1GBASET_DB+
	B-4		PORT114_1GBASET_DB-
	B-5		PORT114_1GBASET_DC+
	B-6		PORT114_1GBASET_DC-
	B-7		PORT114_1GBASET_DD+
	B-8		PORT114_1GBASET_DD-
	C-1		PORT115_1GBASET_DA+
	C-2		PORT115_1GBASET_DA-
	C-3		PORT115_1GBASET_DB+
	C-4		PORT115_1GBASET_DB-
	C-5		PORT115_1GBASET_DC+
	C-6		PORT115_1GBASET_DC-
	C-7		PORT115_1GBASET_DD+
	C-8		PORT115_1GBASET_DD-
	D-1		PORT116_1GBASET_DA+
	D-2		PORT116_1GBASET_DA-
	D-3		PORT116_1GBASET_DB+
	D-4		PORT116_1GBASET_DB-
	D-5		PORT116_1GBASET_DC+
	D-6		PORT116_1GBASET_DC-
	D-7		PORT116_1GBASET_DD+
	D-8		PORT116_1GBASET_DD-

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I/O CHARTS:

I/O CHART (CONTINUED)			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J7 (1GBASE-T) 25-8S KEYING "B"	E-1	BI	PORT117_1GBASET_DA+
	E-2		PORT117_1GBASET_DA-
	E-3		PORT117_1GBASET_DB+
	E-4		PORT117_1GBASET_DB-
	E-5		PORT117_1GBASET_DC+
	E-6		PORT117_1GBASET_DC-
	E-7		PORT117_1GBASET_DD+
	E-8		PORT117_1GBASET_DD-
	F-1		PORT118_1GBASET_DA+
	F-2		PORT118_1GBASET_DA-
	F-3		PORT118_1GBASET_DB+
	F-4		PORT118_1GBASET_DB-
	F-5		PORT118_1GBASET_DC+
	F-6		PORT118_1GBASET_DC-
	F-7		PORT118_1GBASET_DD+
	F-8		PORT118_1GBASET_DD-
	G-1		PORT119_1GBASET_DA+
	G-2		PORT119_1GBASET_DA-
	G-3		PORT119_1GBASET_DB+
	G-4		PORT119_1GBASET_DB-
	G-5		PORT119_1GBASET_DC+
	G-6		PORT119_1GBASET_DC-
	G-7		PORT119_1GBASET_DD+
	G-8		PORT119_1GBASET_DD-
	H-1		PORT120_1GBASET_DA+
	H-2		PORT120_1GBASET_DA-
	H-3		PORT120_1GBASET_DB+
	H-4		PORT120_1GBASET_DB-
	H-5		PORT120_1GBASET_DC+
	H-6		PORT120_1GBASET_DC-
	H-7		PORT120_1GBASET_DD+
	H-8		PORT120_1GBASET_DD-
	A OUTER	--	CHASSIS
	B OUTER		
	C OUTER		
	D OUTER		
	E OUTER		
	F OUTER		
	G OUTER		
	H OUTER		
	SHELL		

Amphenol
MILITARY HIGH SPEED

SOFTWARE

FULLY MANAGED | 60 SECOND BOOT | MANUALS AVAILABLE UPON REQUEST

STACKING
Stacking Ring Topology
Stacking Chain Topology
Removing and Replacing Stacking Members
Exchanging Stacking Members
Switching the Stacking Master

CONFIGURING SYSTEM TIME
Configuring of Daylight Savings Time
Configuring SNTP
Polling for Unicast Time Informaiton
Polling for Anycast Time Information
Broadcast Time Information
Defining SNTP Settings

CONFIGURING DEVICE SECURITY
Configuring Management Security
Configuring Authentication Methods
Defining Access Profiles
Defining Profile Rules
Defining Authenticaion Profiles
Defining RADIOUS Settings
Defining TACACS+ Authentication
Configuring Passwords
Defining Local Users
Defining Line Passwords
Defining Enable Passwords
Configuring Network Security
Network Security Overview
Port-Based Authentication
Advanced Port-Based Authentication
Defining Port Authentication Properties
Defining Port Authentication
Configuring Multiple Hosts
Defining Authentication Hosts
Viewing EAP Statistics
Defining Access Control Lists
Defining IP Based Access Control Lists
Defining MAC Based Access Control Lists
Binding Device Security ACL's
Managing Port Security
Enabling Storm Control

CONFIGURING SYSTEM LOGS
Defining General Log Properties
Viewing Memory Logs
Viewing Flash Logs
Defining System Log Servers

CONFIGURING INTERFACES
Configuring Ports
Aggregating Ports
Configuring LACP
Configuring VLAN's
Defining VLAN Properties
Defining VLAN Membership
Defiing VLAN Interface Settings
Configuring GARP
Defining GARP
Defining GVRP
Viewing GVRP Statistics

DEFINING IP ADDRESSES
Configuring IP Addressing
Defining IP Addressing
Defining ARP
Defining Domain Name Servers
Defining DNS Servers
Defining DNS Host Mapping

DEFINING THE FORWARDING DATABASE
Defining Static Forwarding Database Entries
Defining Dynamic Forwarding Database Entries
CONFIGURING SPANNING TREE
Defining Classic Spanning Tree
Defining STP on Interfaces
Defining Rapid Spanning Tree
Defining Multiple Spanning Tree
Defining MSTP Instances Settings

CONFIGURING SNMP
SNMP v1 and v2c
SNMP v3
Configuring SNMP Security
Defining SNMP View
Defining SNMP Group Profiles
Defining SNMP Group Members
Defining SNMP Communities
SNMP Communities Basic Table
SNMP Communities Advanced Table
Configuring SNMP Notifications
Defining SNMP Notification Global Parameters
Defining SNMP Notificaiton Filters
Defining SNMP Notification Recipients
SNMP v3 Notification Recipients

CONFIGURING MULTICAST FORWARDING
Multicast Forwarding
Typical Multicast Setup
Multicast Operation
Multicast Registration
Multicast Address Properties
Defining Multicast Properties
Adding MAC Group Address
Adding IP Multicast Groups
Configuring IGMP Snooping
Configuring MLD Snooping
Viewing IGMP/MLD IP Multicast Groups
Defining Multicast Router Ports
Defining Forward All Multicast

MANAGING SYSTEM FILES
Downloading System Files
Firmware Download
Configuration Download
Uploading System Files
Upload Type
Software Image Upload
Configuration Upload
Copying Files
Restoring the Defult Configuration File

CONFIGURING QUALITY OF SERVICE
Quality of Service Overview
VPT Classification Information
CoS Services
Defining General QoS Settings
Configuring QoS Settings
Restoring Factory Defult QoS Interface Settings
Defining Queues
Defining Bandwidth Settings
Mapping CoS Values to Queues
Mapping DSCP Values to Queues
Defining QoS Basic Mode
Defiing Basic Mode Settings
Rewritting Basic Mode DSCP Values
Defining QoS Advanced Mode
Setting Policy Binding

MANAGING DEVICE DIAGNOSTICS
Configuring Port Mirroiring

VIEWING STATISTICS
Viewing Interface Statistics
Recieve Statistics
Transmit Statstics
Viewing Etherlike Statistics
Managing RMON Statistics
Viewing RMON Statistics
Configuring RMON History
Defining RMON History Control
Viewing the RMON History Table
Configuring RMON Events
Defining RMON Events Control
Viewing the RMON Events Logs
Defining RMON Alarms

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Amphenol
MILITARY HIGH SPEED

AMPHENOL RUGGEDIZATION DESIGN

OVERVIEW

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications.

TEMPERATURE

Opperating Temperature - thermal cycles between -40ºC and 85ºC while device is operating.

Temperature is measured at chassis housing or card edge

Storage temperature - thermal cycles between -55ºC and 125ºC

HUMIDITY

Operating Humidity - humidity cycle between 0-100% non-condensing humidity while device operating

Storage Humidity - humidity cycle between 0-100% condensing humidity

SEALING

Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION

Sine Vibration - 10g Peak. 5-2,000Hz
- o Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.

Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
- o 60 minutes per axis, in each of three mutually perpendicular axes.

40 G Peak Shock Cycle
- o Three hits in each axis, both directions, 1/2 sine and terminal-leak saw tooth, total 36 hits

FLUID SUSCEPTABILITY

MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE

-1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTROMAGNETIC COMPATIBILITY

Designed to comply with MIL-STL-461E

PRINTED CIRCUIT BOARD ASSEMBLIES

Conformal Coat

Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.

Printed Circuit Board Rigidity

Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3

Printed Circuit Board Fabrication

Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF)

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL- HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

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