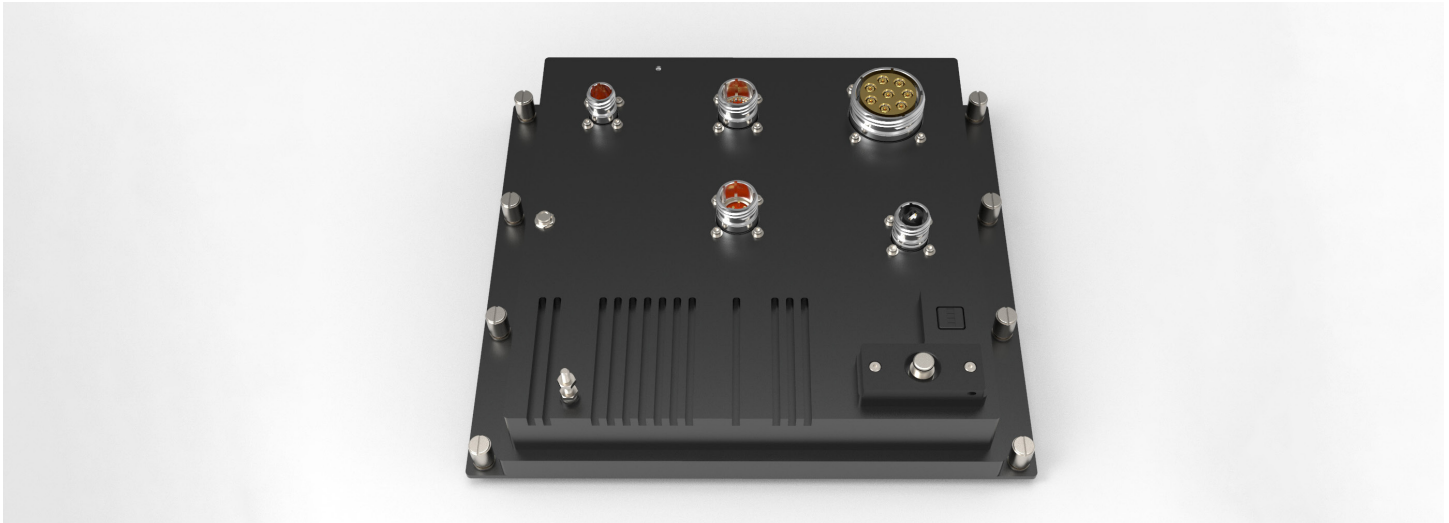


32 CHANNEL 10G ETHERNET SWITCH

HIGH SPEED SOLUTIONS

PDS - 319



Amphenol's Rugged 32 Channel Ethernet Switch Box provides an unmatched level of flexibility to meet any system requirement. The switch box is a 32 port standalone Ethernet Switch box that is configurable for system connectivity, speeds, port types, and interoperability with various high-speed media converters and connectors for system interfacing.

Each port is capable of 10G Ethernet – some ports can either be configured as 10G-Base-T (also supporting 100-Base-T and 1G-Base-T) or 10G-Base-SR and 1G-Base-SX (also supporting 25G Base-SR). The switching throughput is up to 320 Gbps when using all 32 ports on the switch box. In addition, the switch is non-blocking and low-latency for high-throughput architectures and applications. In Amphenol's state of the art Spirent communications testing center, the switch box is tested aggressively at line rates to RFC 2889 for switching and RFC 2544 for L2/L3 performance, latency, packet forwarding, and other key items at full line rate and PRBS 2³¹.

The switch is manufactured using Amphenol's MIL Qualified MIL-DTL-38999 Series III connectors. These connectors contain standard AS39029 qualified Size 22D contacts, Octonet contacts and 48F MT Ferrule Fiber Optic contact assemblies.

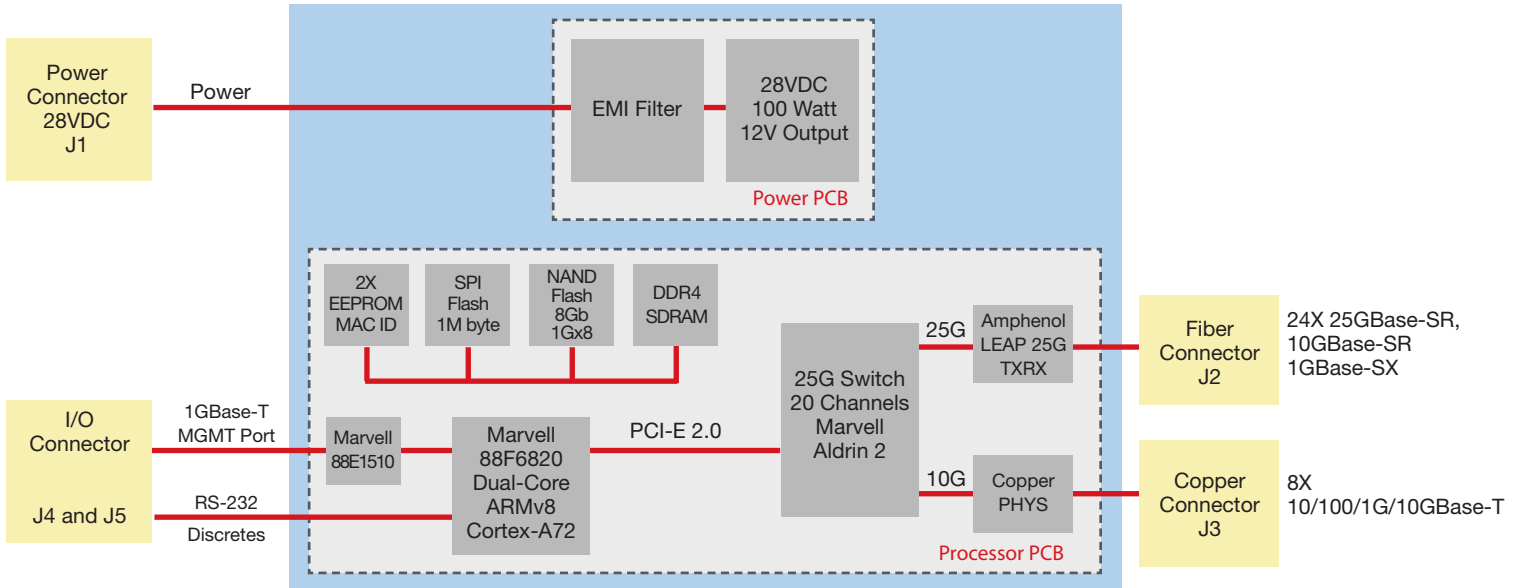
FEATURES AND BENEFITS:

- Eight channels of Copper –
10/100/1G/10GBase-T
- Compliant to IEEE 802.3 and 10GBase-T
- 24 channels of Fiber – configured as
1GBase-SX or 10GBase-SR
- Compliant to IEEE 802.3 Clause 49 & 52
- 320 gigabits per second non-blocking L2/L3 switch
- Dual core ARM processor with flash, SPI, EEPROMs, and DDR3 and mgmt. Ethernet connection
- Uboot and Linux OS for L2 / L3 switching
- Web browser, SSH, CLI, telnet
- Embedded reset and status CPLD
- Support for PTP boundary clock
- Service micro-controller for power down, reset, and restart in overheat event
- 28VDC mil-spec power supply with EMI filter
- 100 Watts typical power consumption at room temperature
- ETI, Circuit breaker, power supply status LEDs
- Power connector, debug connector, maintenance connector – all D38999's
- MIL-Spec black painted chassis with cold plate external conduction cooling
- Environmental requirements nearly identical to current product
- Rear mounting panel is paint free for electrical bonding. The surface is coated with a conductive finish such as alodine or iridite.

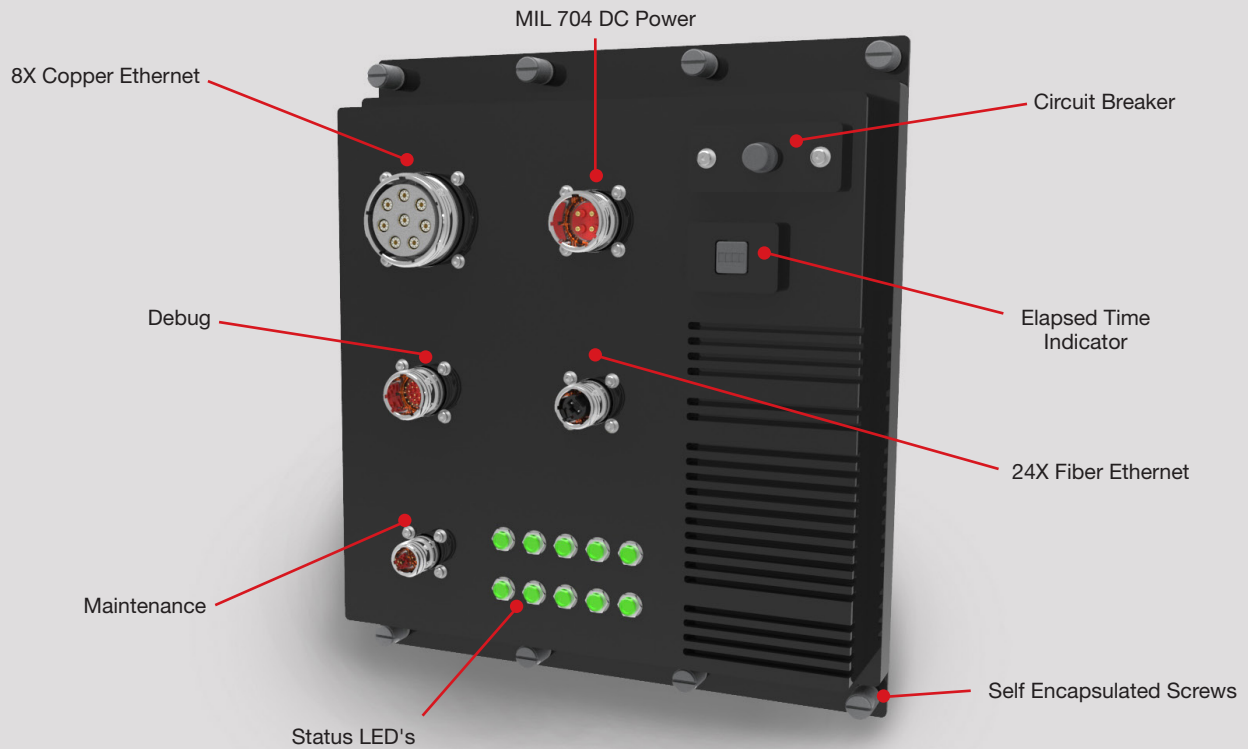
SOFTWARE FEATURES

Stacking	Defining IP Addresses	Managing System Files
Stacking Ring Topology	Configuring IP Addressing	Downloading System Files
Stacking Chain Topology	Defining IP Addresses	Firmware Download
Stacking Members and Unit ID	Defining ARP	Configuration Download
Removing and Replacing Stacking Members	Defining Domain Name Servers	Uploading System Files
Exchanging Stacking Members	Defining DNS Servers	Upload Type
Switching the Stacking Master	Defining DNS Host Mapping	Software Image Upload
Configuring System Time	Defining the Forwarding Database	Configuration Upload
Configuring Daylight Savings Time	Defining Static Forwarding Database Entries	Copying Files
Configuring SNTP	Defining Dynamic Forwarding Database Entries	Restoring the Default Configuration File
Polling for Unicast Time Information	Configuring Spanning Tree	Configuring Quality of Service
Polling for Anycast Time Information	Defining Classic Spanning Tree	Quality of Service Overview
Broadcast Time Information	Defining STP on Interfaces	VPT Classification Information
Defining SNTP Settings	Defining Rapid Spanning Tree	CoS Services
Configuring Device Security	Defining Multiple Spanning Tree	Defining General QoS Settings
Configuring Management Security	Defining MSTP Instance Settings	Configuring QoS General Settings
Configuring Authentication Methods	Defining MSTP Interface Settings	Restoring Factory Default QoS Interface Settings
Defining Access Profiles	Configuring SNMP	Defining Queues
Defining Profile Rules	SNMP v1 and v2c	Defining Bandwidth Settings
Defining Authentication Profiles	SNMP v3	Mapping CoS Values to Queues
Mapping Authentication Methods	Configuring SNMP Security	Mapping DSCP Values to Queues
Defining RADIUS Settings	Defining SNMP Security	Defining QoS Basic Mode
Defining TACACS+ Authentication	Defining SNMP View	Defining Basic Mode Settings
Configuring Passwords	Defining SNMP Group Profiles	Rewriting Basic Mode DSCP Values
Defining Local Users	Defining SNMP Group Members	Defining QoS Advanced Mode
Defining Line Passwords	Defining SNMP Communities	Setting Policy Binding
Defining Enable Passwords	SNMP Communities Basic Table	Managing Device Diagnostics
Configuring Network Security	SNMP Communities Advanced Table	Configuring Port Mirroring
Network Security Overview	Configuring SNMP Notifications	Viewing Statistics
Port-Based Authentication	Defining SNMP Notification Global Parameters .	Viewing Interface Statistics
Advanced Port-Based Authentication	Defining SNMP Notification Filters	Viewing Interface Statistics
Defining Port Authentication Properties	Defining SNMP Notification Recipients	Receive Statistics
Defining Port Authentication	SNMPv1,2c Notification Recipients	Transmit Statistics
Configuring Multiple Hosts	SNMPv3 Notification Recipients	Viewing Etherlike Statistics
Defining Authentication Hosts	Configuring Multicast Forwarding	Managing RMON Statistics
Viewing EAP Statistics	Multicast Forwarding	Viewing RMON Statistics
Defining Access Control Lists	Typical Multicast Setup	Configuring RMON History
Defining IP Based Access Control Lists	Multicast Operation	Defining RMON History Control
Defining MAC Based Access Control Lists	Multicast Registration	Viewing the RMON History Table
Binding Device Security ACLs	Multicast Address Properties	Configuring RMON Events
Managing Port Security	Defining Multicast Properties	Defining RMON Events Control
Enabling Storm Control	Adding MAC Group Address	Viewing the RMON Events Logs
Configuring System Logs	Adding IP Multicast Groups	Defining RMON Alarms
Defining General Log Properties	Configuring IGMP Snooping	
Viewing Memory Logs	Configuring MLD Snooping	
Viewing Flash Logs	Viewing IGMP/MLD IP Multicast Groups	
Configuring Interfaces	Defining Multicast Router Ports	
Configuring Ports	Defining Forward All Multicast	
Aggregating Ports	Defining Unregistered Multicast Settings	
Configuring LACP		
Configuring VLANs		
Defining VLAN Properties		
Defining VLAN Membership		
Defining VLAN Interface Settings		
Configuring GARP		
Defining GARP		
Defining GVRP		
Viewing GVRP Statistics		

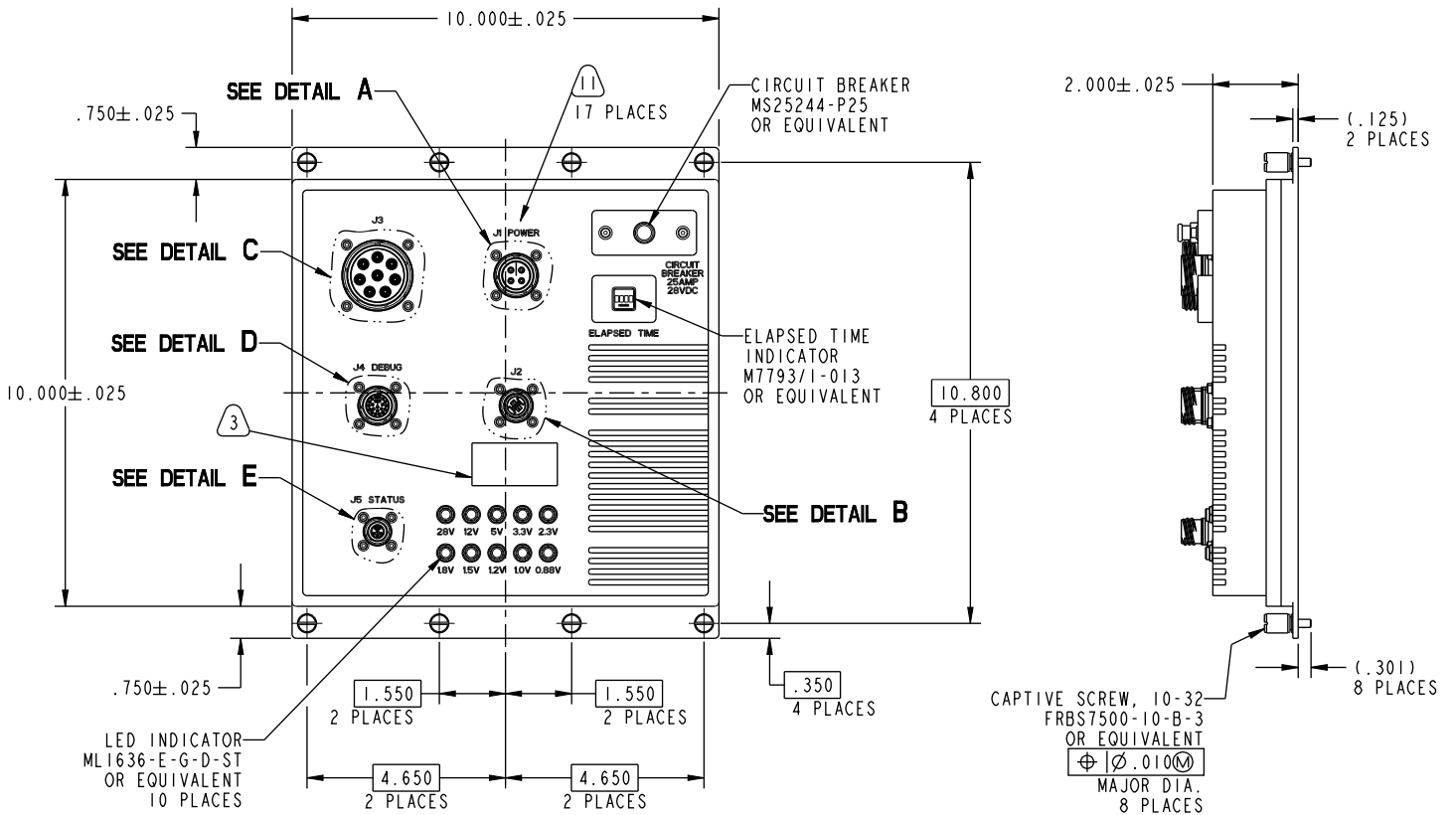
BLOCK DIAGRAM



VISUAL DESCRIPTION

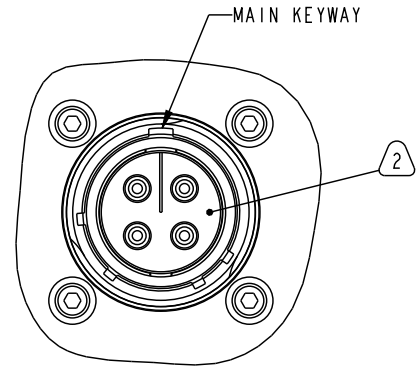


DRAWING

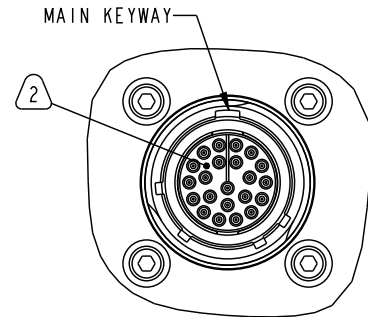


KEY WAY DIAGRAM AND CHART

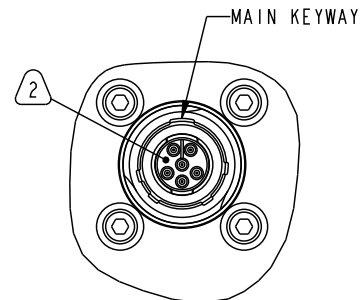
I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	280VDC_IN
	B	OUT	28VDC_RTN
	C	---	SAFETY GROUND / CHASSIS
	D	---	NOT CONNECTED
	SHELL	---	CHASSIS
J4 (DEBUG) 13-35P KEYING "N"	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	IN	DEBUG_JTAG_TCLK
	5	OUT	DEBUG_JTAG_TDO
	6	IN	DEBUG_JTAG_TDI
	7	IN	DEBUG_JTAG_TTMS
	8	IN	DEBUG_I2C_SCL
	9	BI	DEBUG_I2C_SDA
	10	--	NOT CONNECTED
	11	--	NOT CONNECTED
	12	BI	DEBUG_CPU_USB_D+
	13	BI	DEBUG_CPU_USB_D-
	14	BI	DEBUG_CPU_1GBASET_DA+
	15		DEBUG_CPU_1GBASET_DA-
	16		DEBUG_CPU_1GBASET_DB+
	17		DEBUG_CPU_1GBASET_DB-
	18		DEBUG_CPU_1GBASET_DC+
	19		DEBUG_CPU_1GBASET_DC-
	20		DEBUG_CPU_1GBASET_DD+
	21		DEBUG_CPU_1GBASET_DD-
	22	--	NOT CONNECTED
SHELL	--	CHASSIS	
J5 (STATUS/RESET) 9-35P KEYING "N"	1	IN	SWITCHBOX_RESET
	2	OUT	POWERSUPPLY_STATUS
	3	OUT	CHASSIS_STATUS
	4	OUT	TEMPERATURE_WARNING_STATUS
	5	OUT	RESET_RTN
	6	--	NOT CONNECTED
	SHELL	--	SHELL -- CHASSIS



DETAIL A
J1
SCALE 2.000

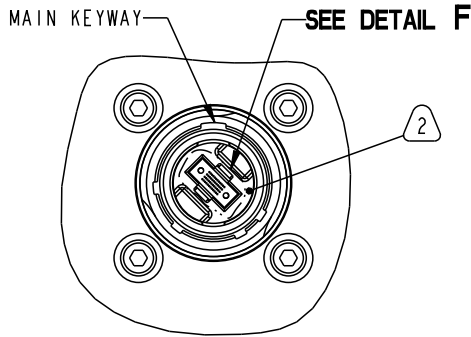


DETAIL D
J4
SCALE 2.000

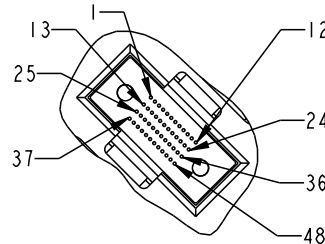


DETAIL E
J5
SCALE 2.000

KEY WAY DIAGRAM AND CHART



DETAIL B
J2
SCALE 2.000

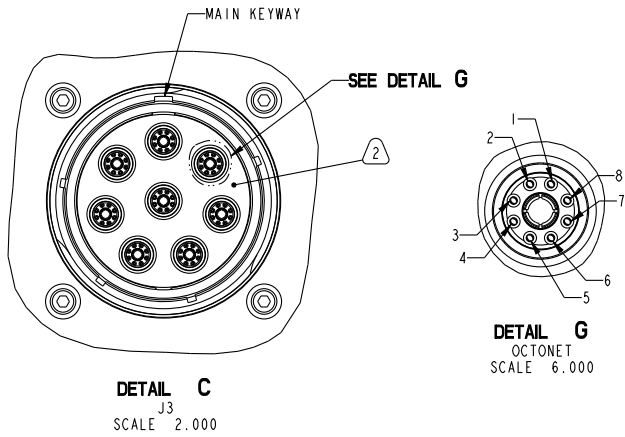


DETAIL F
48F MT
SCALE 6.000

I/O CHART (CONTINUED)			
Connector Description	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 11-1S 48F MT KEYING "N"	1	IN	PORT12_10GBASESR_RX
	2		PORT11_10GBASESR_RX
	3		PORT10_10GBASESR_RX
	4		PORT9_10GBASESR_RX
	5		PORT8_10GBASESR_RX
	6		PORT7_10GBASESR_RX
	7		PORT6_10GBASESR_RX
	8		PORT5_10GBASESR_RX
	9		PORT4_10GBASESR_RX
	10		PORT3_10GBASESR_RX
	11	PORT2_10GBASESR_RX	
	12	PORT1_10GBASESR_RX	
	13	OUT	PORT12_10GBASESR_TX
	14		PORT11_10GBASESR_TX
	15		PORT10_10GBASESR_TX
	16		PORT9_10GBASESR_TX
	17		PORT8_10GBASESR_TX
	18		PORT7_10GBASESR_TX
	19		PORT6_10GBASESR_TX
	20		PORT5_10GBASESR_TX
	21		PORT4_10GBASESR_TX
	22		PORT3_10GBASESR_TX
	23		PORT2_10GBASESR_TX
	24		PORT1_10GBASESR_TX

I/O CHART (CONTINUED)			
Connector Description	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 11-1S 48F MT KEYING "N"	25	IN	PORT24_10GBASESR_RX
	26		PORT23_10GBASESR_RX
	27		PORT22_10GBASESR_RX
	28		PORT21_10GBASESR_RX
	29		PORT20_10GBASESR_RX
	30		PORT19_10GBASESR_RX
	31		PORT18_10GBASESR_RX
	32		PORT17_10GBASESR_RX
	33		PORT16_10GBASESR_RX
	34		PORT15_10GBASESR_RX
	35	PORT14_10GBASESR_RX	
	36	PORT13_10GBASESR_RX	
	37	OUT	PORT24_10GBASESR_TX
	38		PORT23_10GBASESR_TX
	39		PORT22_10GBASESR_TX
	40		PORT21_10GBASESR_TX
	41		PORT20_10GBASESR_TX
	42		PORT19_10GBASESR_TX
	43		PORT18_10GBASESR_TX
	44		PORT17_10GBASESR_TX
	45		PORT16_10GBASESR_TX
	46		PORT15_10GBASESR_TX
	47		PORT14_10GBASESR_TX
	48		PORT13_10GBASESR_TX
SHELL	--		CHASSIS

KEY WAY DIAGRAM AND CHART



I/O CHART (CONTINUED)			
Connector Description	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3 25-8S KEYING "N"	A-1	BI	PORT25_10GBASET_DA+
	A-2		PORT25_10GBASET_DA-
	A-3		PORT25_10GBASET_DB+
	A-4		PORT25_10GBASET_DB-
	A-5		PORT25_10GBASET_DC+
	A-6		PORT25_10GBASET_DC-
	A-7		PORT25_10GBASET_DD+
	A-8		PORT25_10GBASET_DD-
	B-1		PORT26_10GBASET_DA+
	B-2		PORT26_10GBASET_DA-
	B-3		PORT26_10GBASET_DB+
	B-4		PORT26_10GBASET_DB-
	B-5		PORT26_10GBASET_DC+
	B-6		PORT26_10GBASET_DC-
	B-7		PORT26_10GBASET_DD+
	B-8		PORT26_10GBASET_DD-
	C-1		PORT27_10GBASET_DA+
	C-2		PORT27_10GBASET_DA-
	C-3		PORT27_10GBASET_DB+
	C-4		PORT27_10GBASET_DB-
	C-5		PORT27_10GBASET_DC+
	C-6		PORT27_10GBASET_DC-
	C-7		PORT27_10GBASET_DD+
	C-8		PORT27_10GBASET_DD-
	D-1		PORT28_10GBASET_DA+
	D-2		PORT28_10GBASET_DA-
	D-3		PORT28_10GBASET_DB+
	D-4		PORT28_10GBASET_DB-
	D-5		PORT28_10GBASET_DC+
	D-6		PORT28_10GBASET_DC-
	D-7		PORT28_10GBASET_DD+
	D-8		PORT28_10GBASET_DD-

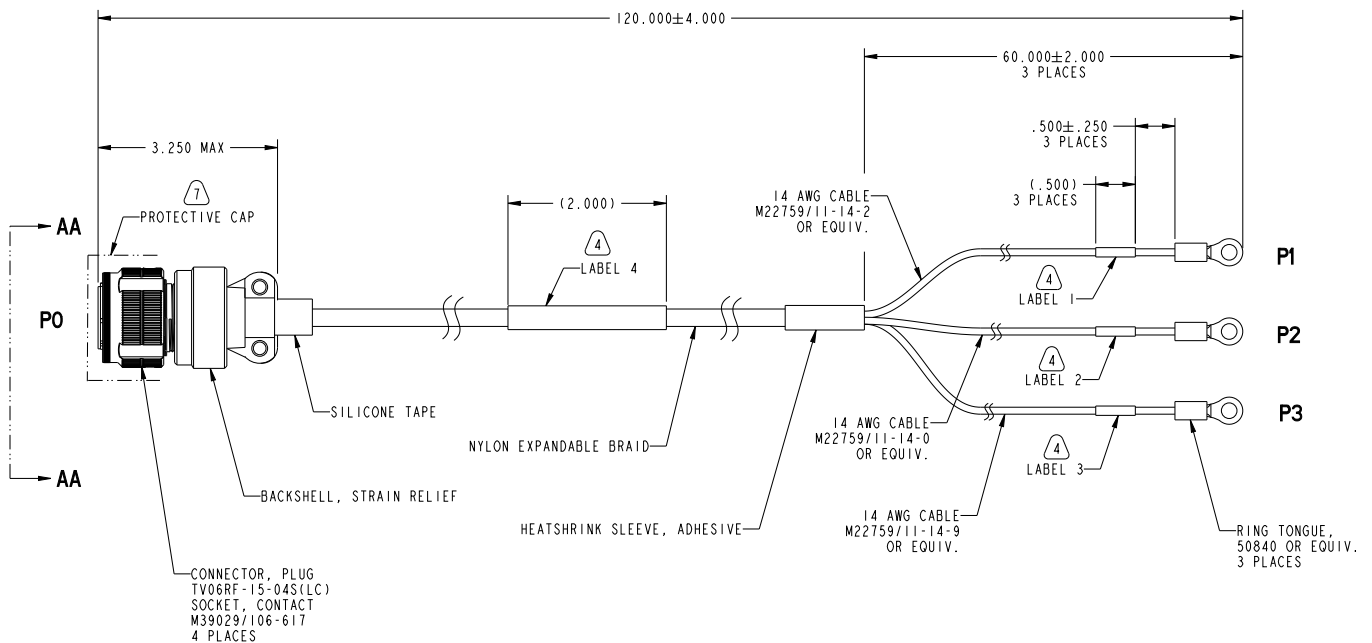
I/O CHART (CONTINUED)			
Connector Description	PIN NO.	DATA DIRECTION	SIGNAL NAME
J3 25-8S KEYING "N"	E-1	BI	PORT29_10GBASET_DA+
	E-2		PORT29_10GBASET_DA-
	E-3		PORT29_10GBASET_DB+
	E-4		PORT29_10GBASET_DB-
	E-5		PORT29_10GBASET_DC+
	E-6		PORT29_10GBASET_DC-
	E-7		PORT29_10GBASET_DD+
	E-8		PORT29_10GBASET_DD-
	F-1		PORT30_10GBASET_DA+
	F-2		PORT30_10GBASET_DA-
	F-3		PORT30_10GBASET_DB+
	F-4		PORT30_10GBASET_DB-
	F-5		PORT30_10GBASET_DC+
	F-6		PORT30_10GBASET_DC-
	F-7		PORT30_10GBASET_DD+
	F-8		PORT30_10GBASET_DD-
	G-1		PORT31_10GBASET_DA+
	G-2		PORT31_10GBASET_DA-
	G-3		PORT31_10GBASET_DB+
	G-4		PORT31_10GBASET_DB-
	G-5		PORT31_10GBASET_DC+
	G-6		PORT31_10GBASET_DC-
	G-7		PORT31_10GBASET_DD+
	G-8		PORT31_10GBASET_DD-
	H-1		PORT32_10GBASET_DA+
	H-2		PORT32_10GBASET_DA-
	H-3		PORT32_10GBASET_DB+
	H-4		PORT32_10GBASET_DB-
	H-5		PORT32_10GBASET_DC+
	H-6		PORT32_10GBASET_DC-
	H-7		PORT32_10GBASET_DD+
	H-8		PORT32_10GBASET_DD-
A OUTER		--	CHASSIS
B OUTER			
C OUTER			
D OUTER			
E OUTER			
F OUTER			
G OUTER			
H OUTER			
SHELL			

CONNECTOR LIST

CONNECTOR LIST				
CONNECTOR DESIGNATOR	CONNECTOR PART NUMBER	CONTACT(S) USED	MATING CONNECTOR (OR EQUIVALENT)	MATING CONTACT (OR EQUIVALENT)
J1 POWER	CF-971354-04P	4X) SIZE 12 PIN M39029/107-623	V06RF-15-4S(LC)	SIZE 12 SOCKET M39029/106-617
J2	CF-971332-01S	(1X) 48F MT FERRULE 12599 (1X) MT MALE KIT CF-198233-001	CF-594611-01P	48F MT FERRULE 12599 MT FEMALE KIT CF-198234-001
J3	10-646402-612N	8X) 21-032907-001 OCTONET, SOCKET	TV06RQF-25-8P(LC)	21-032904-021 OCTONET, PIN COMPATIBLE W/ PIC E6A3824 100OHM CABLE (OR EQUIVALENT)
J4 DEBUG	CF-971353-22P	(22X) SIZE 22D PIN M39029/107-620	V06RF-13-35S(LC)	SIZE 22D SOCKET M39029/106-614
J5 STATUS	CF-971351-35P	(6X) SIZE 22D PIN M39029/107-620	TV06RF-9-35S(LC)	SIZE 22D SOCKET M39029/106-614

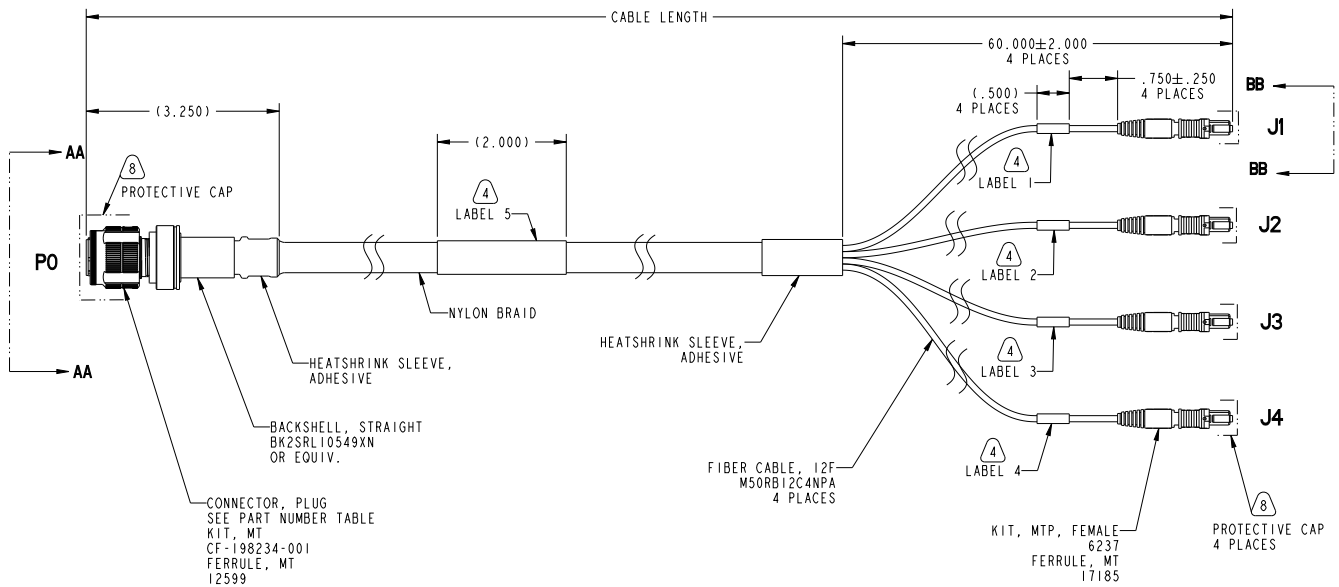
POWER TEST CABLE CA-628485-G08 FOR J1

J1 Insert Drawing and pinout from CA-628485-G08



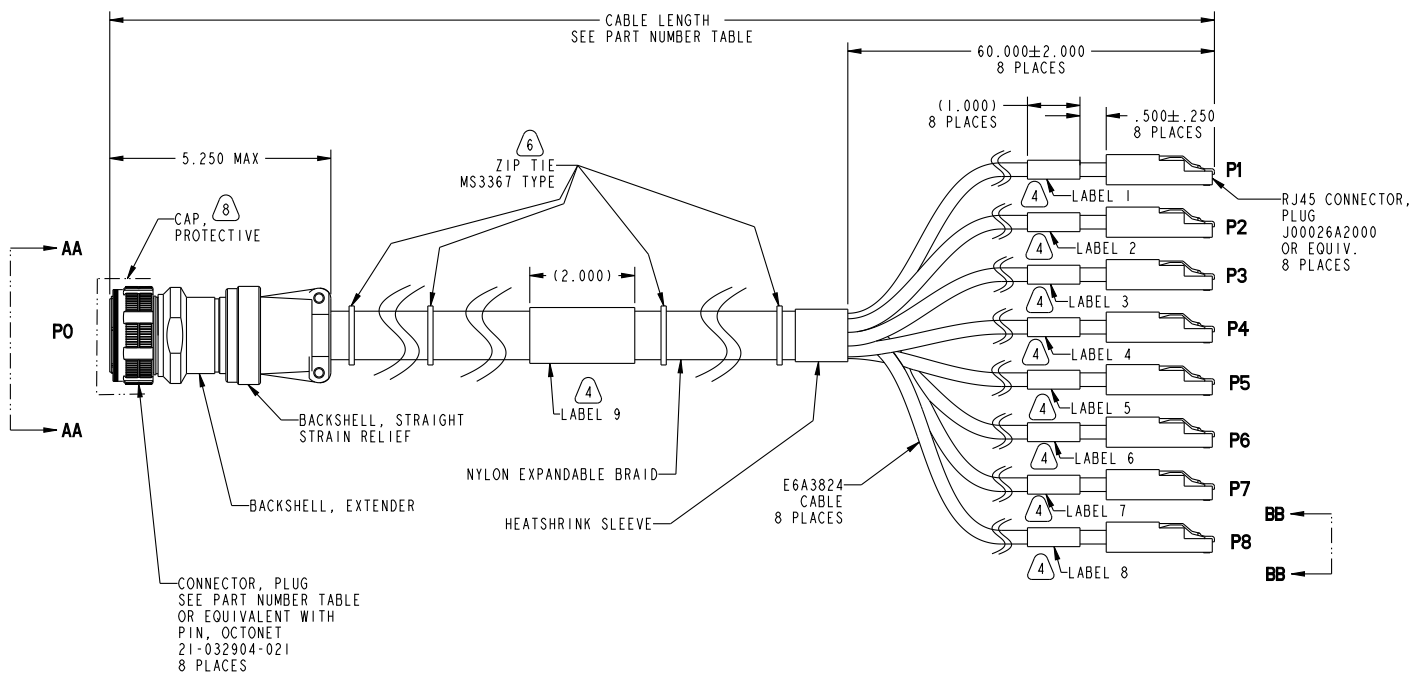
FIBER TEST CABLES CF-980062-10X FOR J2

J2 Insert Drawing and pinout from CF-980062-101



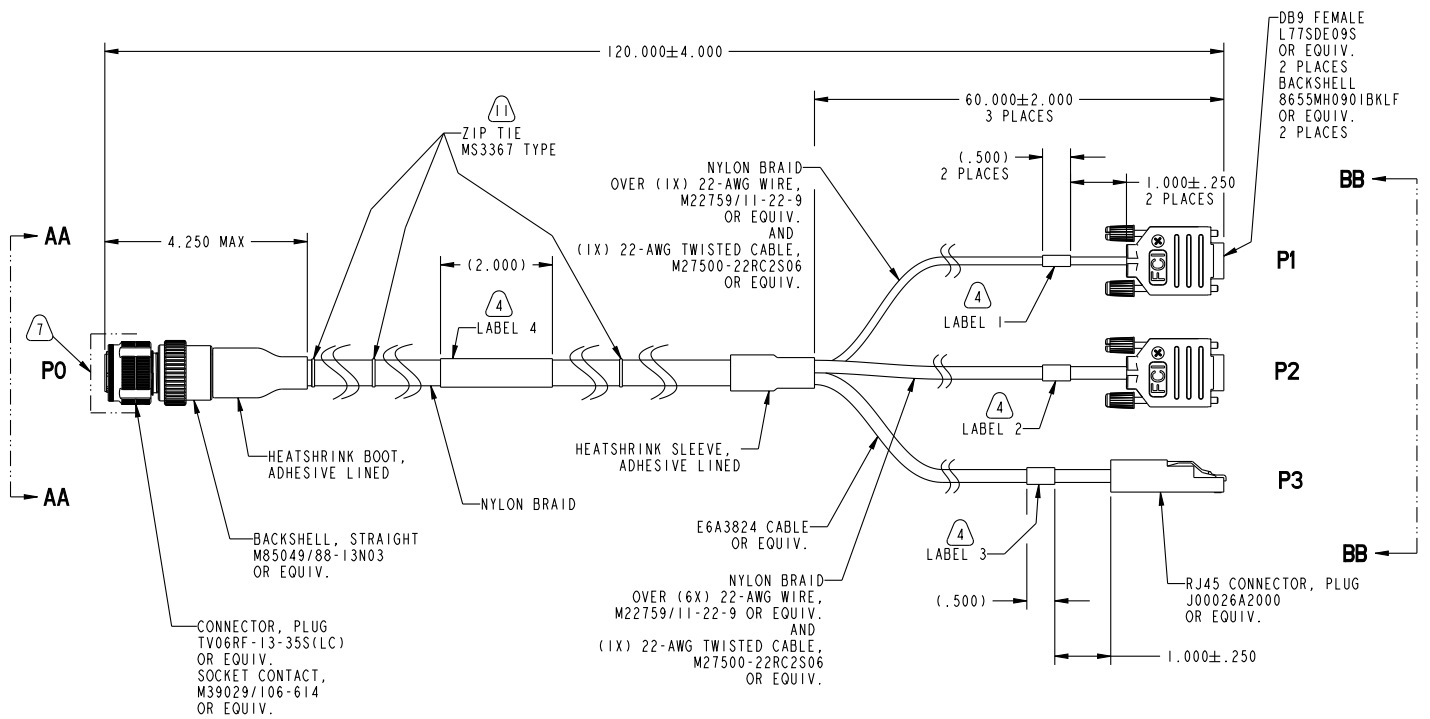
ETHERNET TEST CABLE CA-628485-G09 FOR J3

J3 Insert Drawing and pinout from CA-628485-G09



DEBUG TEST CABLE CA-628485-G11 FOR J5

J5 Insert Drawing and pinout from CA-628485-G11



MAINTENANCE TEST CABLE CA-628485-G10 FOR J4

J4 Insert Drawing and pinout from CA-628485-G10

