

Amphenol Aerospace

CF-020400-026

Thermal Analysis Update 2

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Objectives

1. Determine how the CF-170200-233 board performs with the frame [CF-0200400-026] for conduction cooling for the following environments and fixed temperatures on the side surfaces of the secondary frame:

a) -40°C

b) 23°C

c) 85°C

At the three different power levels:

a) Sandia Config. – Total Power of 37.93W

b) 10G Op. - Total Power of 61.12W

c) Worst-case – Total Power of 87.91W

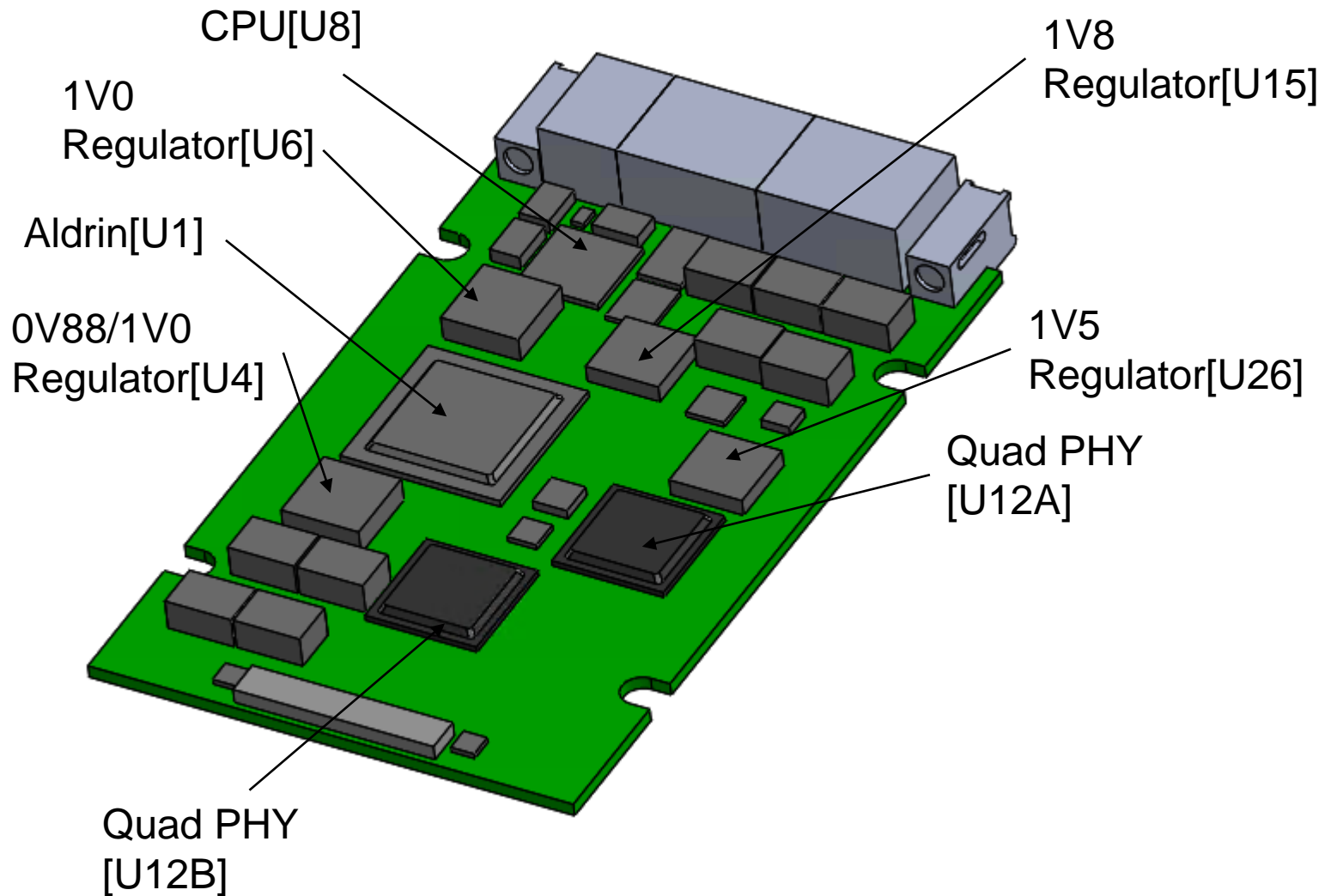
2. Generate recommendations to improve thermal performance.

Updates

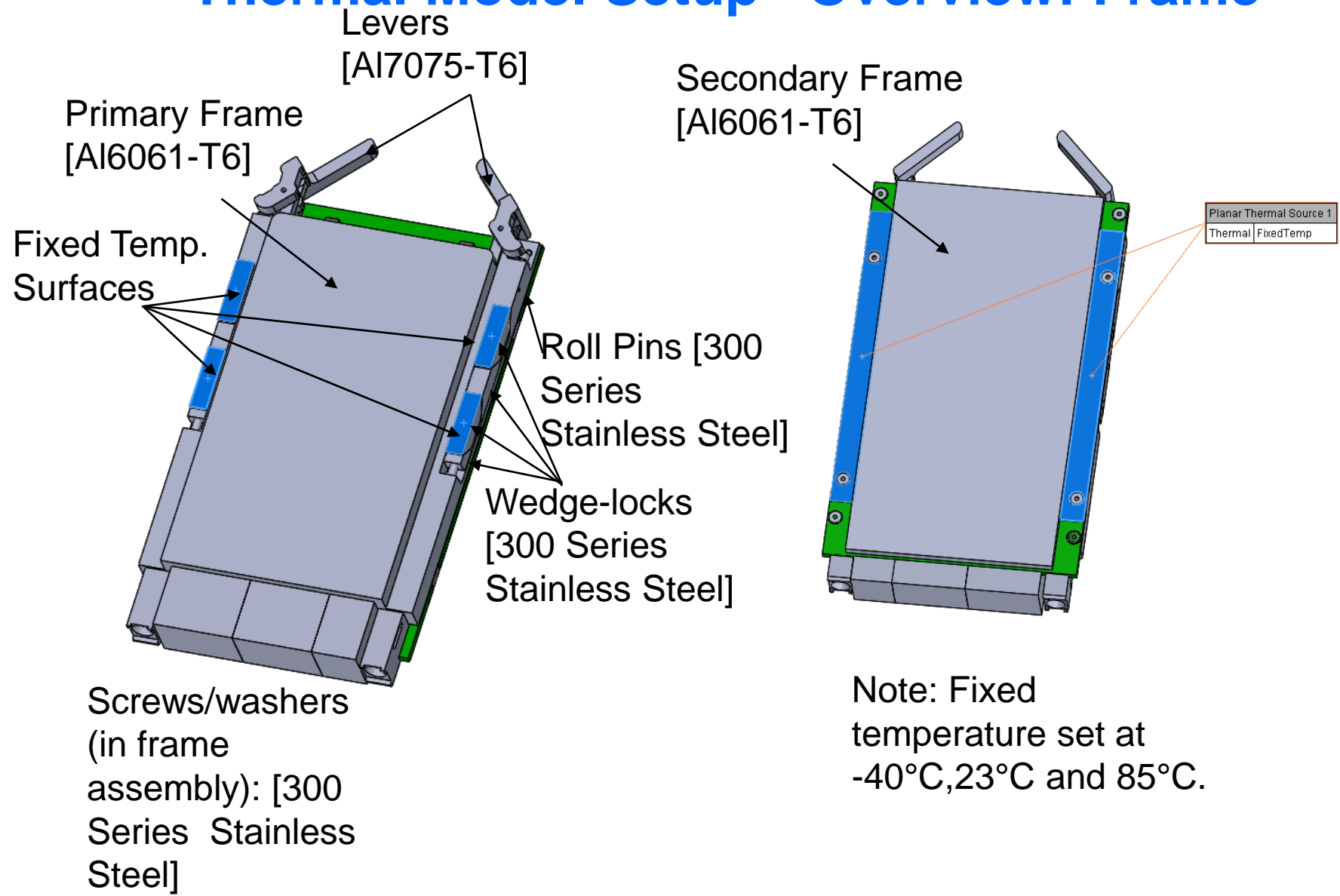
1. The updates for this thermal model are based on changes on the CAD model provided, cf-020400-026m__asm_010720.stp and includes the following:
 - a) The primary frame was revised to remove fins above the Aldrin and increase pedestal heights to allow for thinner gap pads on the critical components.
 - b) The thermal gap pads on the primary frame coupled to the critical components are SilPad2000 with $k=3.5\text{W/mK}$ at 0.015" thick (was: Therm-A-Gap 579, $k=3\text{W/mK}$, 0.2" thick). This was also used to couple surfaces between frames.
 - c) The thermal gap pad on the secondary frame coupled to the secondary side (bottom) of the PCB is Gap Pad V0 Ultra Soft with $k=1\text{W/mK}$, 0.1" thick.
 - d) Additional cooling surfaces (fixed temperature surfaces) on the top surfaces of the wedges were added.

Thermal Model Setup

Thermal Model Setup –Overview: Board

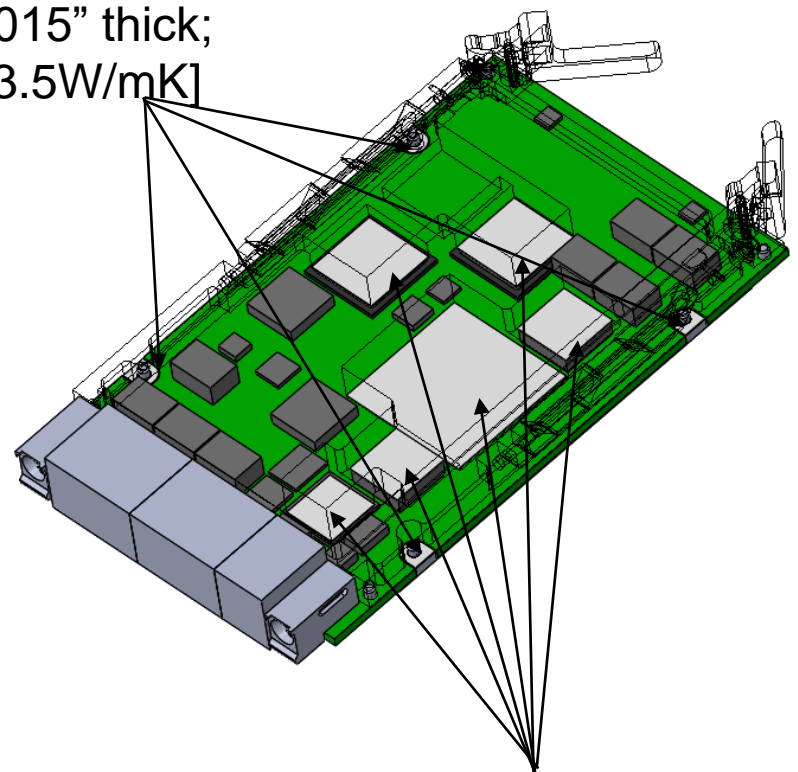


Thermal Model Setup –Overview: Frame

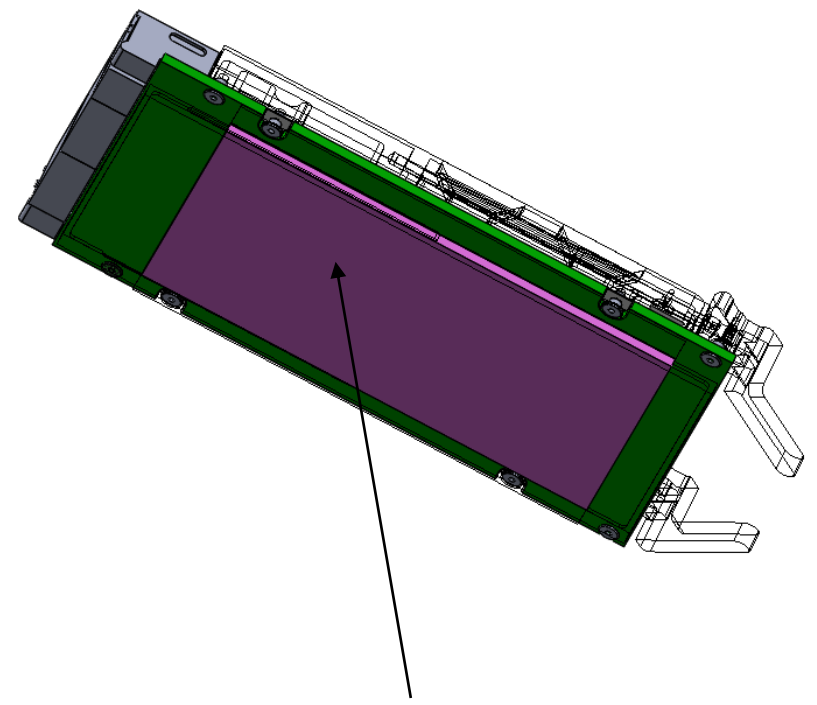


Thermal Model Setup –Overview: Thermal Gap Pads

Thermal Gap Pads
(SilPad2000)
[0.015" thick;
 $k=3.5\text{W/mK}$]



Thermal Gap Pads
(SilPad2000)
[0.015" thick; $k=3.5\text{W/mK}$]



Thermal Gap Pad (Gap
Pad V0 Ultra Soft)
[0.1" thick; $k=1\text{W/mK}$]

Thermal Data

CF-170300-233	Sandia Config. (W)			Thermal Resistance (°C/W)/Model		Maximum Temperature (°C)
Component [Ref. Des.]	Qty	Per Component	Total	R _{JC}	R _{JB}	
Aldrin [U1]	1	20.5	20.50	0.16	1.72	110 (junction)
CPU [U8]	1	4.67	4.67	2.57	6.89	115 (junction)
Quad PHY [U12A,U12B]	2	4.2	8.40	0.3	2.6	105 (junction)
0V88 / 1V0 Regulator [U4]	1	2.05	2.05	3.7	1.5	125 (junction)
1V0 Regulator [U6]	1	0.6	0.60	3.7	1.5	125 (junction)
1V8 Regulator [U15]	1	0.11	0.11	5	2	125 (junction)
1V5 Regulator [U26]	1	0.19	0.19	5	2	125 (junction)
Spread on the Board (Misc.)	1	1.41	1.41			
		Total	37.93			

CF-170300-233	10G Op.(W)			Thermal Resistance (°C/W)/Model		Maximum Temperature (°C)
Component [Ref. Des.]	Qty	Per Component	Total	R _{JC}	R _{JB}	
Aldrin [U1]	1	23.18	23.18	0.16	1.72	110 (junction)
CPU [U8]	1	4.67	4.67	2.57	6.89	115 (junction)
Quad PHY [U12A,U12B]	2	13.12	26.24	0.3	2.6	105 (junction)
0V88 / 1V0 Regulator [U4]	1	2.32	2.32	3.7	1.5	125 (junction)
1V0 Regulator [U6]	1	1.52	1.52	3.7	1.5	125 (junction)
1V8 Regulator [U15]	1	0.12	0.12	5	2	125 (junction)
1V5 Regulator [U26]	1	0.59	0.59	5	2	125 (junction)
Spread on the Board (Misc.)	1	2.48	2.48			
		Total	61.12			

Note: Thermal resistances from junction to case (R_{JC}) and from junction to board (R_{JB}) and thermal limits were taken from “Parts Thermal Characteristics.pdf”. Items in red were based on typical values for a similar package (15 Ld QFN).

Thermal Data (continued)

CF-170300-233	Worst-case Power (W)			Thermal Resistance (°C/W)/Model		Maximum Temperature (°C)
	Component [Ref. Des.]	Qty	Per Component	Total	R _{JC}	
Aldrin [U1]	1	43	43.00	0.16	1.72	110 (junction)
CPU [U8]	1	7.8	7.80	2.57	6.89	115 (junction)
Quad PHY [U12A,U12B]	2	13.5	27.00	0.3	2.6	105 (junction)
0V88 / 1V0 Regulator [U4]	1	4.3	4.30	3.7	1.5	125 (junction)
1V0 Regulator [U6]	1	1.74	1.74	3.7	1.5	125 (junction)
1V8 Regulator [U15]	1	0.22	0.22	5	2	125 (junction)
1V5 Regulator [U26]	1	0.61	0.61	5	2	125 (junction)
Spread on the Board (Misc.)	1	3.24	3.24			
		Total	87.91			

Note: Thermal resistances from junction to case (R_{JC}) and from junction to board (R_{JB}) and thermal limits were taken from “Parts Thermal Characteristics.pdf”. Items in red were based on typical values for a similar package (15 Ld QFN).

Thermal Analysis

Results Summary

Scenario					Thermal-026		Thermal-026		Thermal-026	
Parameters										
Wedges and Secondary Frame Surfaces Fixed Temp., °C					-40		23		85	
Remarks					Sandia Config.		Sandia Config.		Sandia Config.	
RESULTS										
Component [Ref. Des]	Power, W	Min. Limit, °C	Max. Limit, °C	Limit Type	Result, °C	Margin, °C	Result, °C	Margin, °C	Result, °C	Margin, °C
Aldrin [U1]	20.5	-40	110	junction	-18.5	128.5	44.0	66.0	105.7	4.3
CPU [U8]	4.67	-	115	junction	-15.8	130.8	46.8	68.2	108.5	6.5
Quad PHY [U12A]	4.2	-	105	junction	-26.5	131.5	36.2	68.8	98.0	7.0
Quad PHY [U12B]	4.2	-	105	junction	-26.0	131.0	36.7	68.3	98.5	6.5
0V88 / 1V0 Regulator [U4]	2.05	-40	125	junction	-27.4	152.4	35.4	89.6	97.2	27.8
1V0 Regulator [U6]	0.6	-40	125	junction	-28.5	153.5	34.3	90.7	96.1	28.9
1V8 Regulator [U15]	0.11	-	125	junction	-33.8	158.8	29.1	95.9	91.1	33.9
1V5 Regulator [U26]	0.19	-	125	junction	-35.7	160.7	27.2	97.8	89.2	35.8

Scenario					Thermal-026		Thermal-026		Thermal-026	
Parameters										
Wedges and Secondary Frame Surfaces Fixed Temp., °C					-40		23		85	
Remarks					10G Op.		10G. Op.		10G Op.	
RESULTS										
Component [Ref. Des]	Power, W	Min. Limit, °C	Max. Limit, °C	Limit Type	Result, °C	Margin, °C	Result, °C	Margin, °C	Result, °C	Margin, °C
Aldrin [U1]	23.18	-40	110	junction	-10.9	120.9	51.5	58.5	113.1	-3.1
CPU [U8]	4.67	-	115	junction	-10.3	125.3	52.2	62.8	113.9	1.1
Quad PHY [U12A]	13.12	-	105	junction	-11.9	116.9	50.5	54.5	112.1	-7.1
Quad PHY [U12B]	13.12	-	105	junction	-11.0	116.0	51.4	53.6	113.0	-8.0
0V88 / 1V0 Regulator [U4]	2.32	-40	125	junction	-22.3	147.3	40.4	84.6	102.2	22.8
1V0 Regulator [U6]	1.52	-40	125	junction	-22.5	147.5	40.1	84.9	101.9	23.1
1V8 Regulator [U15]	0.12	-	125	junction	-31.0	156.0	31.8	93.2	93.8	31.2

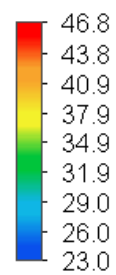
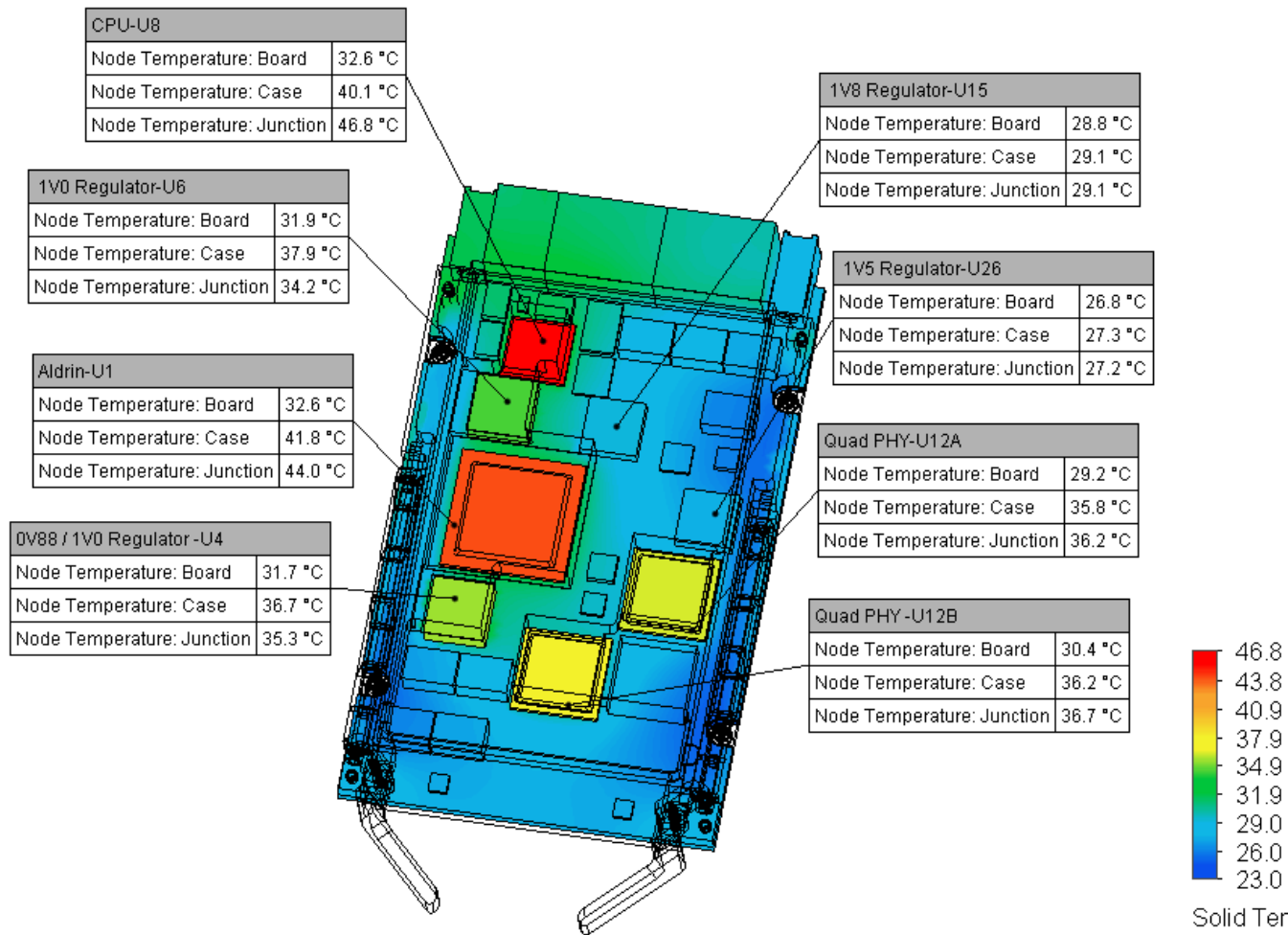
- For the Sandia Config. and 85°C, Aldrin has a 4°C margin.

Results Summary (continued)

Scenario					Thermal-026		Thermal-026		Thermal-026	
Parameters										
Wedges and Secondary Frame Surfaces Fixed Temp., °C					-40		23		85	
Remarks					Worst-Case Power		Worst-Case Power		Worst-Case Power	
RESULTS										
Component [Ref. Des]	Power, W	Min. Limit, °C	Max. Limit, °C	Limit Type	Result, °C	Margin, °C	Result, °C	Margin, °C	Result, °C	Margin, °C
Aldrin [U1]	43	-40	110	junction	7.0	103.0	69.0	41.0	130.3	-20.3
CPU [U8]	7.8	-	115	junction	7.0	108.0	69.2	45.8	130.6	-15.6
Quad PHY [U12A]	13.5	-	105	junction	-5.0	110.0	57.3	47.7	118.8	-13.8
Quad PHY [U12B]	13.5	-	105	junction	-3.7	108.7	58.6	46.4	120.0	-15.0
0V88 / 1V0 Regulator [U4]	4.3	-40	125	junction	-12.0	137.0	50.5	74.5	112.1	12.9
1V0 Regulator [U6]	1.74	-40	125	junction	-14.1	139.1	48.3	76.7	109.9	15.1
1V8 Regulator [U15]	0.22	-	125	junction	-26.3	151.3	36.4	88.6	98.4	26.6
1V5 Regulator [U26]	0.61	-	125	junction	-29.0	154.0	33.8	91.2	95.8	29.2

Board Surface Temperature Plot

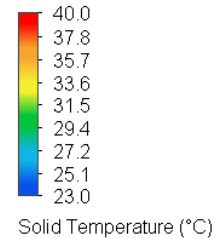
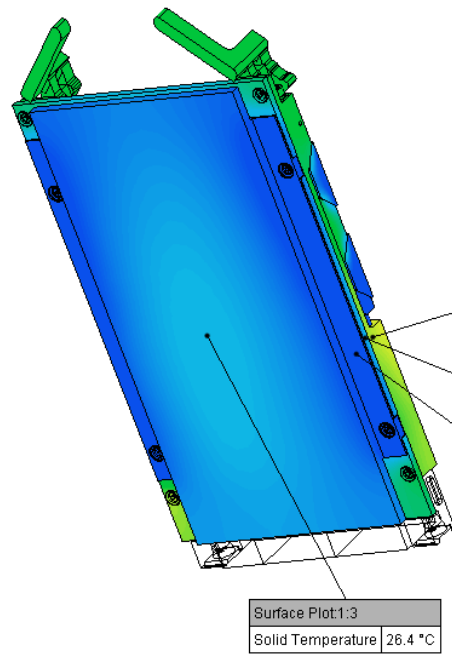
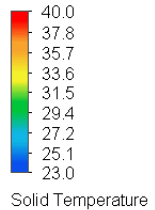
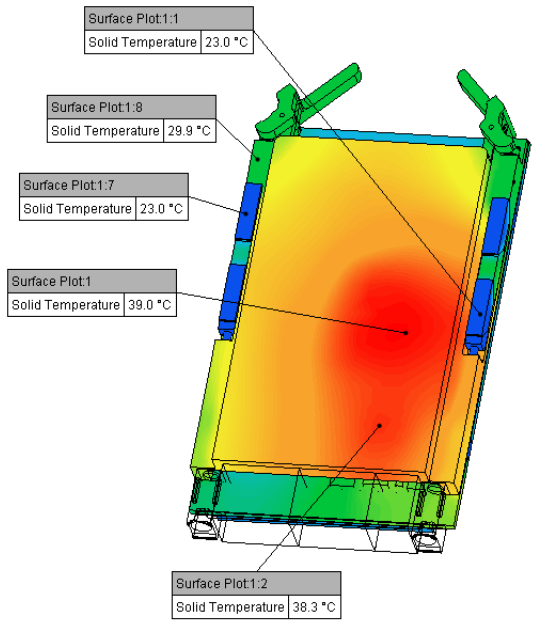
Sandia Config., 23°C



Solid Temperature (°C) 14

Frame/Board Surface Temperature Plot

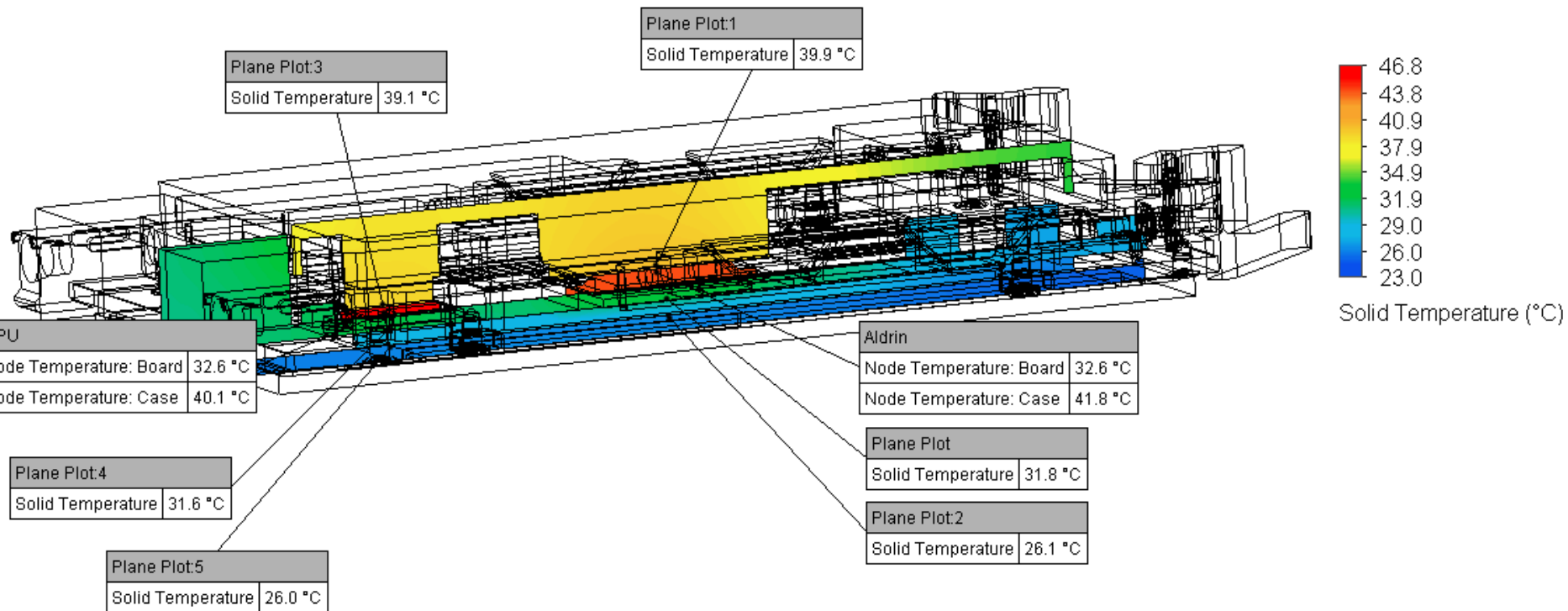
Sandia Config., 23°C



- There is a 9°C temperature gradient from the secondary frame to the primary frame which is a 5°C decrease compared to the baseline.

Cutplane Temperature Plot: Mid-width of Aldrin

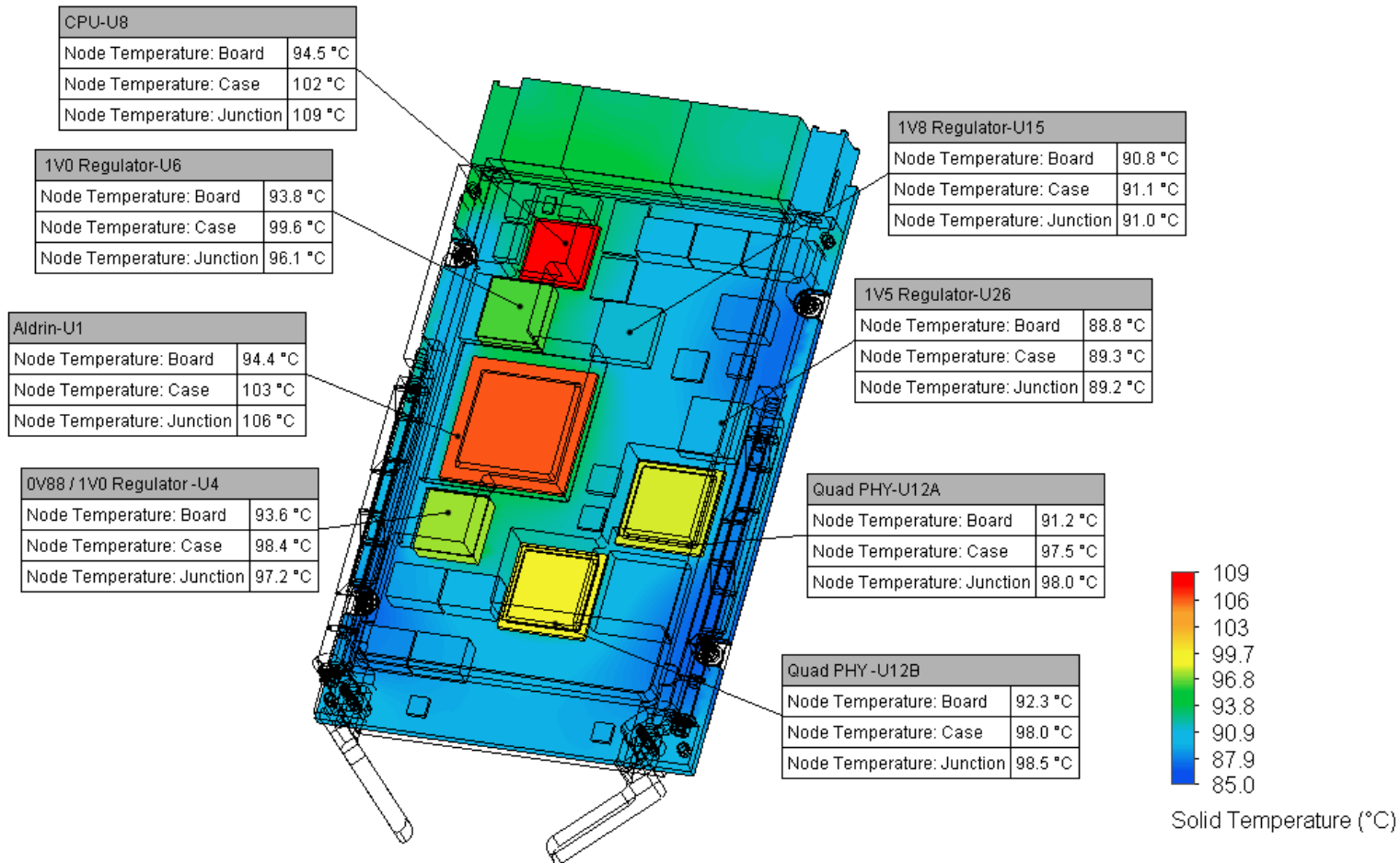
Sandia Config., 23°C



- There is a 2°C temperature gradient from the Aldrin top case to the primary frame.
- There is a 1°C temperature gradient from the CPU top case to the primary frame.
- These temperature gradients are significantly lower than the baseline.
- There is a 6°C temperature gradient from the board to the secondary frame that can be improved with a higher thermal conductivity gap pad.

Board Surface Temperature Plot

Sandia Config., 85°C



Recommendations

- The reduction in the thickness of the thermal gap pads for the Aldrin, CPU and Quad PHYs improved the junction temperatures such that all critical components are within their limits for Sandia Config. at the maximum operating temperature of 85°C. Implementation of this is highly recommended.
- Consider a higher thermal conductivity thermal gap pad (say $k=3\text{W/mK}$) coupling the PCB to the secondary frame to further improve the critical component temperatures.
- The contact areas between the primary frame and the secondary frame ideally must be increased. The addition of thermal gap pads on the contact areas between the primary and secondary frames helped reduce the temperature gradient between the two frames.
- For the 10G Op., the Quad PHYs exceed their limit by as much as 8°C at 85°C. It is recommended to limit the operating temperature to 70°C for this power scenario.
- For worst-case power, the Aldrin is 20°C over the limit at 85°C. It is recommended to limit the operating temperature for this scenario with this current configuration to 60°C.