ESD Attenuation Test Procedure for Connectors with Faraday Cage Protective Structures

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Engineering Document

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Scope

To characterize the voltage and current developed on the contacts of a connector (which has Faraday cage protective structures) when ESD events occur at the connector mating interface. The ESD events shall be air discharge type events to determine if the faraday cage precludes direct discharges to the contacts, and direct discharges to the faraday cage to determine the maximum voltage and current induced on the contacts.

Note: This test assumes that the connector under test need only provide ESD protection in its unmated state. The Faraday cage protective structures will provide little to no protection if contacts are probed or if a cable is mated to the protected connector and a discharge is conducted down the cable into the connector.

The original design was developed to protect LRM connectors from the effects of ESD. Since then, the scope has been increased to include MS cylindrical connectors with crimp contacts, and EMI filter pin connectors. These ESD protected connectors are available in aluminum and composite materials, qualified to MIL-C-38999 Rev. J.

For further information on ESD Protected connectors or any of the other products in the Amphenol family of interconnection products, contact:

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1.0 Conditions

1.1. Unless otherwise specified, testing shall be conducted under any combination within the ranges below:

Temperature: 20°C to 30°C

Relative Humidity: 10% to 80%

Barometric Pressure: 550 to 800 mmHg

2.0 Samples

2.1 Samples shall be mounted to a shielded enclosure which shall contain the measurement equipment and all associated cabling and probes. The samples shall be mounted in the manner intended for general use; no supplementary grounding devices shall be permitted. Components such as heatsinks and covers, which are usually provided by the customer, shall be included if they are an integral part of the ESD protection scheme.

LRM type connectors shall be mounted to a heatsink board package, and their surface mount tails soldered to a test board as shown in Figure 1. A contact from each row shall be terminated to an isolated pad at one end and at the center of the insert (8 contacts total). All other contacts shall be terminated to a common trace which shall be connected to the heatsink and connector shell. See Figure 2 for the test board layout. After the connector has been mounted and the probe interfaces attached (socket contacts), the probe interfaces shall be bonded to the test board via epoxy. The surface mount leads and solder pads may be coated IAW MIL-I-46058, type UR, if desired, to minimize internal connector discharges.

If desired, surge arresting devices may be connected between the probe interfaces and the common ground trace or between the two probe tips to minimize the chance of overloading the oscilloscope/combiner. The surge arresters should be characterized to insure that they do not suppress signals which are within the measurement range of the oscilloscope and probe combination.

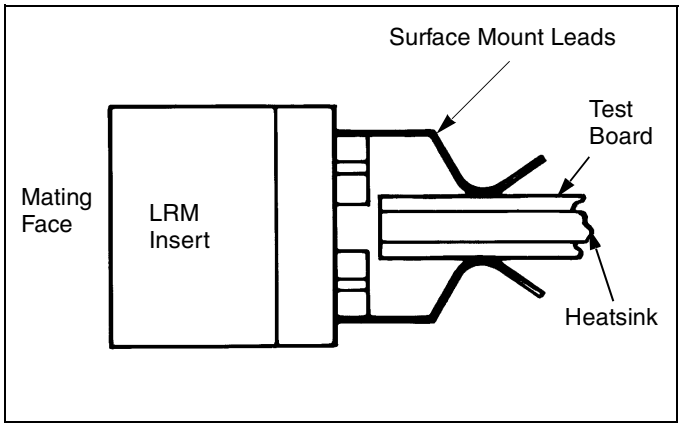

Figure 1
End View of an LRM Insert
Mounted to a Heatsink-Board Package

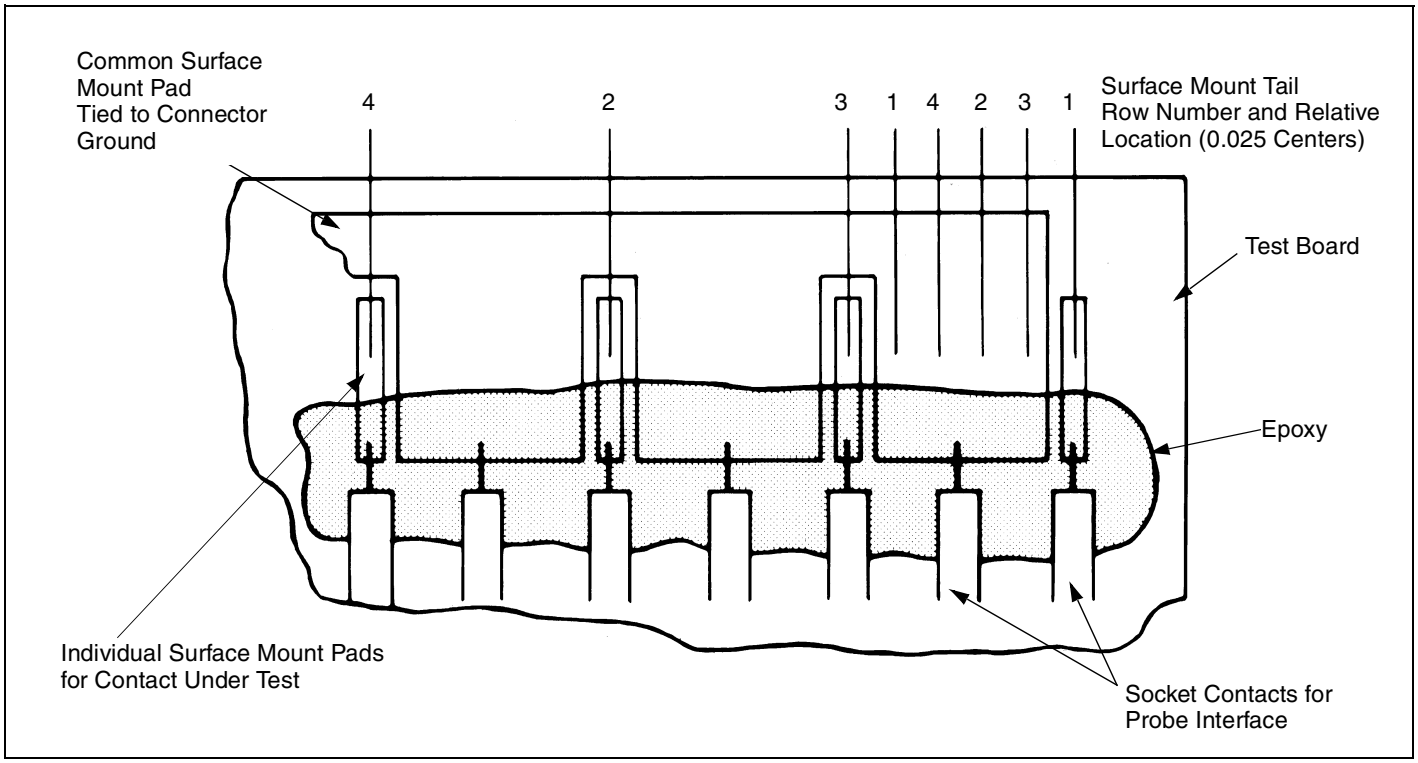

Figure 2
Test Board Layout

3.0 Equipment

3.1 Oscilloscope

3.1.1 The oscilloscope shall have an analog bandwidth of 500 MHz. A digital storage oscilloscope (DSO) is preferred, and if used shall have a sampling rate of at least 2 GS/s.

3.2 ESD Simulator

3.2.1 The simulator shall be designed to meet the discharge requirements of MIL-STD-883D, Method 3015.7. The discharge network shall be a capacitance of 100 pF and a resistance of 1500 Ω, unless otherwise specified. The voltage range shall be ±1 to 25 KV for both air and direct discharges (minimum). The air discharge probe geometry shall be a .5 inch diameter sphere, and the direct discharge probe shall come to a sharp point.

3.3. Voltage Probes

3.3.1 The voltage probes shall have a minimum analog bandwidth of 500 MHz. The use of dual probes is preferred to minimize distortion due to electrical noise (utilizing common mode rejection). Probe input impedance shall be 450 Ω minimum, unless otherwise specified.

When the faraday cage attenuation factor is unknown, and voltage levels are high, the Balanced Coaxial Probe is the probe of choice. This probe can be custom designed to both provide a large amount of attenuation and handle high voltages. Details of the construction of such a probe can be found in proceedings of the 1992 EOS/ESD Symposium or in “High Frequency Measurements and Noise in Electronic Circuits” by Douglas C. Smith (Van Nostrand Reinhold publisher). The probe factor should be adjusted to minimize the chance of a voltage exceeding the safe limit of the oscilloscope (for a 50 Ω input impedance most scopes cannot take more than 5 VRMS).

Once the voltage level has been determined, standard oscilloscope voltage probes with an analog bandwidth greater than 500 MHz and an input impedance of 1 M Ω (or greater) are preferred and should be used if possible.

3.4 Current Probes

3.4.1 The current probes shall have an approximate bandwidth of 300 MHz. The probe input impedance shall be between 1 and 50 Ω (from the contact under test to the heatsink). The probe of choice is the Coaxial Current Probe. Details of the construction of such a probe can be found in proceedings of the 1992 EOS/ESD Symposium or in “High Frequency Measurements and Noise in Electronic Circuits” by Douglas C. Smith (Van Nostrand Reinhold publisher).

4.0 Test Set Up

4.1 The connector under test shall be mounted to a shielded enclosure, in which the measurement equipment shall reside as shown in Figure 3. AC power coming into the shielded enclosure shall be filtered to minimize the noise conducted into the oscilloscope. The voltage probe common shield (if using the Balanced Coaxial Probe) shall be connected to the heatsink of the sample under test. The current probe shield (if using the Coaxial Current Probe) shall be connected to the heatsink of the sample under test.

The shielded room or enclosure shall be closed prior to any electrostatic discharges

5.0 Calibration of Measurement System

5.1 Voltage Probe/Common Mode Rejection Calibration

5.1.1 When using a probing system which utilizes common mode rejection to enhance the signal to noise ratio the voltage probes and/or the oscilloscope must be calibrated to maximize the common mode rejection.

5.1.1.1 If the oscilloscope used has the ability to skew the channels relative to each other via a calibration mode, the following process should be followed:

1. Attach the voltage probe/probes to the two oscilloscope channels to be used.
2. Connect both voltage probe tips to a common square wave such as that at the calibrator output of the oscilloscope.
3. Select one of the channels as the trigger source, and using edge trigger mode adjust the trigger level until a stable, triggered display for each channel is present.
4. If available, turn averaging on (16 samples).
5. Set the vertical scale on each channel so the traces fill as much of the screen as possible without being clipped.
6. Adjust the vertical offset as necessary to align the two traces vertically. If necessary, adjust the probe attenuation value on one channel at regions of the signal where the slope is zero until the waveforms overlap (adjust the time base scale accordingly to view zero slope portions of the signal).
7. Set the time base scale to 500 ps/div.

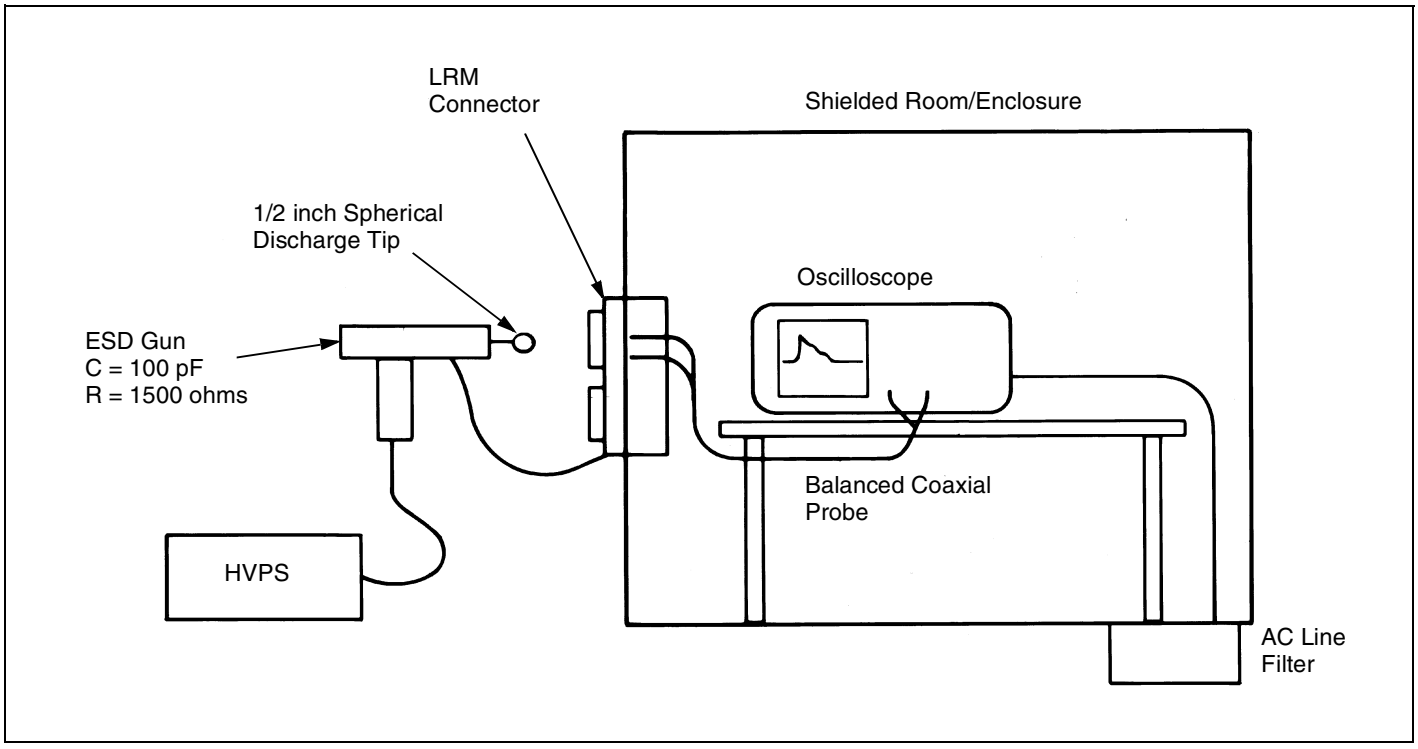

Figure 3
Test Set Up

8. On the channel which is not used for the trigger, adjust the skew so the two channels overlap each other at the fastest-slewing portion of the edge.
9. Create a math function waveform which subtracts one of the channels from the other.
10. Adjust the vertical scale of the math function to be 1/10 of the scale of the channels.
11. Adjust the probe attenuation ratio for minimum deflection in the areas of the waveform where the slope is zero. Ignore the fast slewing portion of the waveform when making these adjustments (the time base scale may have to be increased to 5 ns/div to better see the zero slope portions of the waveform).

Note: This calibration procedure was taken from a Hewlett Packard application note, number 1221 “Differential Measurements on Wideband Signals”.

5.1.2 When using the Balanced Coaxial Probe with a two-way, 180° power combiner to provide the common mode rejection, the combiner should have a bandwidth of at least 500 MHz. The following procedure should be followed to insure maximum common mode rejection:

1. Connect the probe/probes to the two way 180° combiner and the combiner to the desired oscilloscope channel.
2. Connect the two probe tips together (beyond the terminating resistor) and connect the shields of the probes to a ground plane.
3. Discharge an appropriate voltage square wave into the probe tips (appropriate determined by attenuation factor of the probes). The square wave should have a risetime of no greater than 3 ns. An excellent square wave source is a transmission line pulser.
4. Observe the waveform displayed on the scope, and determine the peak voltage. Use this voltage and the probe factor to determine the amount of common mode rejection in decibels:

   Common Mode Rejection

   (dB)=20*log((V*A)/Vin)

   Where:

   Vin = Square-wave input voltage

   V= Peak voltage observed on the scope

   A= Attenuation factor of probe (calculated)
5. Repeat steps 1 through 4 with the probes reversed on their input to the combiner.

6. The probe/combiner combination which gives the best common mode rejection ratio should be marked and used. One should expect the common mode rejection to be at most -25dB, depending on the combiner used. If it is greater than -20dB for both combinations, check the probes for defects and repair and retest as necessary.

Note: This calibration procedure was based on the input from Doug Smith during his presentation at the 1992 EOS/ESD symposium entitled "Fast Transient/EMI Measurements". Smith referred to such a calibration as a "null experiment" for his Balanced Coaxial Probe.

5.2 Current Probe Calibration/Characterization

5.2.1. The Coaxial Current Probe shall be mounted to a shielded enclosure. The joint between the outer conductor of the Coaxial Current Probe and the shielded enclosure should not exceed 2 m Ω. Initially, the current probe shall be attached directly to the oscilloscope. If the voltage measured by the oscilloscope approaches 5V during testing, a 20 dB attenuator should be used to connect the probe to the oscilloscope. After the probe has been connected as described above, the calibration shall proceed as follows:

1. A square wave of 500 V magnitude shall be directly discharged into the tip of the Coaxial Current Probe five times. Record the peaks and risetimes, and plot one waveform. The risetime of the square wave should not exceed 3 nanoseconds.
2. Step 1 shall be repeated at 1000, 2000, and 4000 V.
3. The peaks of each waveform shall be converted from volts to amps (without attenuation I=V; with 20 dB attenuation I=(V)10), averaged and plotted for each Coaxial Current Probe, which can be used to predict the current created by different voltage discharges.

   If a Transmission Line Pulser (TLP) is used to create the square waves then the following relationship can be used to calculate the expected current:

   Expected Current =
   Voltage/Source Impedance of TLP

   A Transfer Impedance can then be assigned to each Coaxial Current Probe by dividing the average measured current by the Expected Current for each voltage. The smallest Transfer Impedance value should be assigned to the probe.

   All unknown signals measured with the Coaxial Current Probe shall be divided by the Transfer Impedance to convert them into actual values.

Note: A calibration procedure for an inductive type current probe has yet to be developed.

5.3 System Voltage Calibration

5.3.1 After probe calibration has been completed a calibration of the voltage measurement system shall be conducted as follows:

1. The voltage probes shall be connected to the oscilloscope as determined by the voltage probe calibration (par. 5.1), with the oscilloscope and probes located within the shielded enclosure as shown in Figure 3.
2. The voltage probe tip shall be extended through the wall of the shielded room, and the ground lead attached to the wall. This connection shall seal the aperture in the shielded room as best as possible.

Note: When using the Balanced Coaxial Probe, the common shield of the probe shall be attached to the shielded room wall at 360°, and the second probe tip attached outside of the shielded room.

3. An appropriate voltage square wave shall be discharged into the probe tip. The voltage level shall be determined by the attenuation of the probe being tested. Record the peaks and risetimes for five square wave pulses, and plot one waveform. The risetime of the square waves shall not exceed 3 nanoseconds.
4. Step 3 shall be repeated at three additional voltage levels, encompassing the range of the probe.
5. The data obtained shall be plotted and used to establish the true voltage attenuation factor of the "system".

5.4 ESD Simulator Calibration

5.4.1 The Coaxial Current Probe shall be mounted to a shielded enclosure as described in paragraph 5.2.1. The oscilloscope analog bandwidth shall be set to 100 MHz. The ESD simulator should be fitted with the direct discharge probe (sharp tip). The ESD Simulator Calibration shall proceed as follows:

1. The ESD simulator shall be charged to +500

V (+1000 V if +500 V is not possible) and direct/contact discharged into the tip of the Coaxial Current Probe five times, recording the peaks and risetimes, and plotting one waveform.

2. Step 1 shall be repeated at +1000, +2000, +4000, +5000, +10000, +15000, +20000, +25000, -500, -1000, -2000, -4000, -5000, -10000, -15000, -20000, and -25000 V.
3. The five peak readings for each voltage shall then be averaged, and the average divided by the transfer impedance of the probe to convert to actual current values.

The waveforms should be compared to those found in MIL-STD-883, Method 3015.7. The peak current should meet or exceed the specified limits (risetime should be less than 10 nanoseconds); peak to peak ringing should not exceed 33% of the peak current. For those voltages not listed in the MIL-STD, the peak current should be meet or exceed I=V/1500.

If the current peak is less than what was expected, additional testing must be done. A calibration chart must be created which lists the target voltage, target current, and corresponding voltage setting on the ESD simulator. During all subsequent testing, the chart shall be used to set the ESD simulator voltage in order to test for the target voltage.

6.0 Test Definition

6.1 ESD Air Discharge Test

6.1.1 The air discharge test determines the maximum voltage and current imparted on the contacts of a connector protected with a faraday cage structure during air discharges to the connector mating face.

The ESD test shall be conducted as follows:

1. The test probes shall be calibrated as defined in paragraph 5.1 and 5.2.
2. The measurement system and ESD simulator shall be calibrated as defined in paragraphs 5.3 and 5.4.
3. The connector under test shall be mounted as defined in paragraph 2.1. The probes shall be connected to the contacts under test (see figure 2 for suggested method of connection). Optimally two sets of voltage and current probes would be used; one of each would be connected to a contacts at the center of the insert and the other two connected to a contacts at the end of the insert to capture information at two areas of the connector under test for each discharge.

   Optionally, the groups of four contacts may be ganged together and connected to individual probes.
4. Each of the contacts under test shall then be subjected to either the System Voltage or Current Probe Calibration (par. 5.3 or 5.2), and the data compared to the original calibrations to insure that the sample has not adversely effected the measurement system.

   This can be accomplished by injecting the square waves on a mating contact which has been carefully inserted into the connector to isolate it from the faraday cage.
5. The shielded enclosure shall be closed.
6. The ESD simulator shall be equipped with the.5 inch diameter air discharge probe. The ESD simulator shall then be charged to the +500 VDC (if possible) and discharged into the mating surface of the connector insert at the end near the contacts under test. The discharge shall be accomplished by charging the simulator away from the test sample then quickly moving the simulator to the position on the connector under test until contact is achieved. This shall be done at least five times, recording the peaks and risetimes, and plotting one waveform.

   False triggering may occur when the trigger of the ESD simulator is first actuated, instead of capturing the effects of the actual discharge. The only way to confirm this is by observation (unless your DSO has a gigantic memory). The best way to avoid this problem is to use delayed triggering. It can also be accomplished by arming the DSO trigger after the ESD simulator trigger has been actuated; however the delay associated with this may bleed the ESD simulator's actual voltage to a lower value than necessary.

   If no signal can be detected (after searching with both positive and negative slope) document that voltage was less than the value of the ground noise and move to the next voltage.
7. Repeat step 6 except discharge into the center or away from the contacts under test in the insert.

8. Repeat steps 4 through 7 moving the probes to different rows on the connector until all rows have been characterized (4 rows for the LRM connector based on symmetry; one group of 4 contacts at the end of the insert and another group of 4 contacts at the center. Center and end are relative to the longest axis of the insert).
9. Repeat steps 5 through 8 for 1000V, 2000V, 3000V, 4000V, 5000V, 10000V, 15000V, 20000V and 25000V.
10. The ESD simulator shall then be charged to -500 VDC (if possible) and discharged into the mating surface of the connector insert at the end as in step 6. This shall be done at least 5 times, recording the peaks and risetimes and plotting one of the waveforms.
12. Repeat step 10 except discharge into the center or away from the contacts under test in the insert.
11. Repeat steps 5 through 8 for -1000V, -2000V, -3000V, -4000V, -5000V, -10000V, -15000V, -20000V and -25000V.
12. Repeat the calibration (step 2) at the end of each testing session to insure that the measurement system parameters have not changed.

6.2 ESD Direct Discharge Test

6.2.1 The direct discharge test shall be used to determine the worse case maximum current and voltage which can be induced on contacts when a 25000V ESD event is intentionally discharged into the faraday cage structure.

After completing steps 1 through 5 of paragraph 6.1.1 initiate the following test sequence:

1. Install the sharp-tipped, direct discharge probe on the ESD simulator.
2. Set the ESD simulator to direct discharge mode. Charge the simulator to +25000 V.
3. Place the tip of the discharge probe on the faraday cage near the contact under test at the mating face of the connector. Discharge the ESD simulator five times, recording the peaks and risetimes of each, and plotting one of the waveforms.
4. Place the tip of the discharge probe on the faraday cage away from the contact under test at the mating interface. Discharge the ESD simulator five times, recording the peaks and risetimes of each, and plotting one of the waveforms.
5. Repeat for all 8 contact locations until both current and voltage data has been collected for each location.
6. Repeat steps 3 through 5 with the ESD simulator set at -25000 V.